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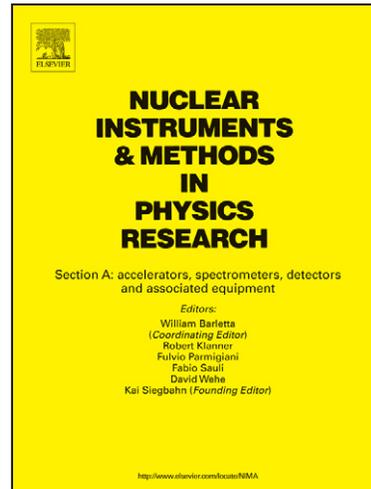
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Fabrication of back-illuminated, fully depleted charge-coupled devices

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Abstract

We describe a fabrication strategy to produce fully depleted, back-illuminated charge-coupled devices (CCDs). Wafers are partially processed at a commercial foundry using standard processing techniques. The wafers are then thinned to the final desired thickness, and the processing steps necessary to produce back-illuminated devices are performed in our laboratory. The CCDs are then probed at wafer level, and we describe our techniques to screen for gate insulator flaws as well as defects on the back side of the wafer that are important for fully depleted devices.

Key words: charge-coupled device, fully depleted, high resistivity silicon, back illuminated, fabrication techniques
PACS: 85.30.De, 85.40.-e, 85.60.Gz

1. Introduction

Large format, scientific charge-coupled devices (CCDs) are the detector of choice for imaging and spectroscopy at UV and visible wavelengths for ground- and space-based astronomy. For wide-field imaging it is necessary to have a large focal plane consisting of arrays of scientific CCDs. As an example of an existing camera, the MegaCam imager at the Canada-France-Hawaii Telescope consists of 40, 2048 \times 4162 (13.5 μm pixel) CCDs [1]. Larger focal plane arrays are proposed, including the Subaru Telescope HyperSuprime camera with plans for 176 2048 \times 4096 (15 μm pixel) CCDs [2], and the Large Synoptic Survey Telescope camera where approximately 200 imagers are required [3].

In order to achieve this major increase in pixel counts, it is necessary to develop robust CCD fabrication methods that result in high yield. Cost is a consideration given that the present-day price of scientific CCDs is approximately \$50–100k per 2k \times 4k CCD.

In this work we describe fabrication techniques used at the Lawrence Berkeley National Laboratory (LBNL) to fabricate scientific CCDs. The CCDs de-

veloped at LBNL are fabricated on high-resistivity silicon, and as a result, relatively thick, fully depleted devices are realized [4]. We have demonstrated that the processing necessary to produce back-illuminated CCDs can be done at the wafer level and in batches of multiple wafers. This allows for high throughput and good repeatability since the processing steps are done nearly simultaneously for the batch.

2. Fully depleted CCD operating principles and fabrication

Figure 1 a) shows a cross-sectional drawing generated from the process simulation program TSUPREM4 [5] of the fully depleted, back-illuminated CCD described in this work. The CCD thickness, typically 200–300 μm , results in improved near-infrared response when compared to standard scientific CCDs that are thinned to 20 μm thickness and below. The CCDs are fully depleted by the use of a substrate bias voltage. This results in a spatial resolution that can be controlled via CCD thickness, substrate bias voltage, and operating

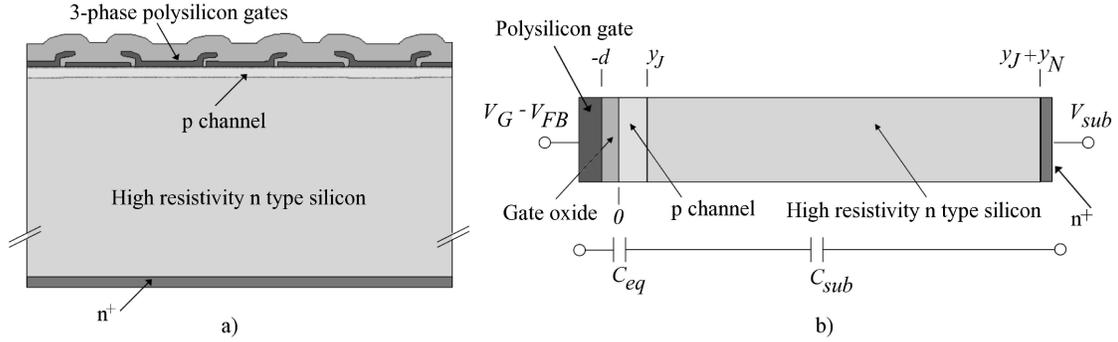


Fig. 1. a) Cross-sectional drawing of the CCD described in this work. The cross section was generated by the process simulator TSUPREM4 [5]. b) Simplified cross section and the equivalent circuit.

temperature. Figure 1 b) shows a simplified cross section and an equivalent circuit. Since the substrate capacitance $C_{sub} = \epsilon_{Si}/y_N$ for a thick device is much less than C_{eq} , the series combination of the p channel and gate insulator capacitance, the substrate bias voltage has little effect on the potential in the CCD channel. y_N is the substrate thickness and ϵ_{Si} is the permittivity of silicon. Therefore this type of CCD can be operated over a wide range of substrate bias voltages, and we have demonstrated operation of both 200 and 650 μm thick CCDs at voltages as high as 200V [6].

The buried-channel, three-phase CCD is fabricated in a 150 mm wafer, triple-polysilicon process with a minimum feature size of 2.5 μm . Most of the fabrication is done at a commercial foundry (DALSA Semiconductor). The advantages of working with a commercial foundry include fast turnaround, good repeatability from run to run, access to a large number of process steps, and economies of scale.

However, fabrication of back-illuminated CCDs requires deviations from typical silicon processing. Science requirements often dictate a wafer thickness that is not the same as the standard wafer thickness used in the foundry. For example, spatial resolution requirements for the SuperNova Acceleration Probe [7] require a wafer thickness of approximately 200 μm , which is to be compared to the standard 150 mm wafer thickness of 675 μm . Such a wide range of thickness usually exceeds the limits over which standard photolithography equipment can achieve proper focus. Also, in our experience 200 μm thick, 150 mm wafers are fairly robust to breakage, but some care is required in wafer handling. Because of these considerations we have found it necessary to develop in-house the technologies necessary to

produce fully depleted, back-illuminated CCDs.

The fabrication work at LBNL is done at the MicroSystems Laboratory (MSL), a Class 10 clean room. The wafers are processed through 8 of the 11 photomasking steps at DALSA Semiconductor. A small number of wafers are then completed at DALSA Semiconductor for quality control purposes, with the remaining wafers sent to our laboratory. The latter are then sent to a commercial vendor where they are thinned to the desired final thickness. In addition to thinning, the wafer back sides are polished to a prime wafer finish at this step. Since the thinned wafers will go through photolithography steps, it is a requirement that the wafers be sufficiently flat after the thinning process. We typically achieve a total thickness variation of 8 μm or better after thinning, which is compatible with the 12 μm depth of focus for the projection aligner used at LBNL.

After thinning, the wafers are returned to LBNL and a thin in-situ doped polysilicon (ISDP) layer is deposited to form the back side n+ contact shown in Fig. 1. This layer must be thin for good blue and UV response and also must be able to tolerate full depletion without an increase in dark current. The typical thickness is 20–25 nm. This layer is deposited by low-pressure, chemical-vapor deposition at 650°C in a horizontal reactor furnace.

The thin ISDP layer is then removed from the front surface of the wafer by plasma etching and the first lithography step is performed on the thinned wafers. In order to match the lithography equipment at the commercial foundry, alignment verniers are included at 4 locations on the wafer. Layer to layer registration measurements are taken on the verniers, and alignment errors including translation, magnification, and skew can be corrected. Once this is

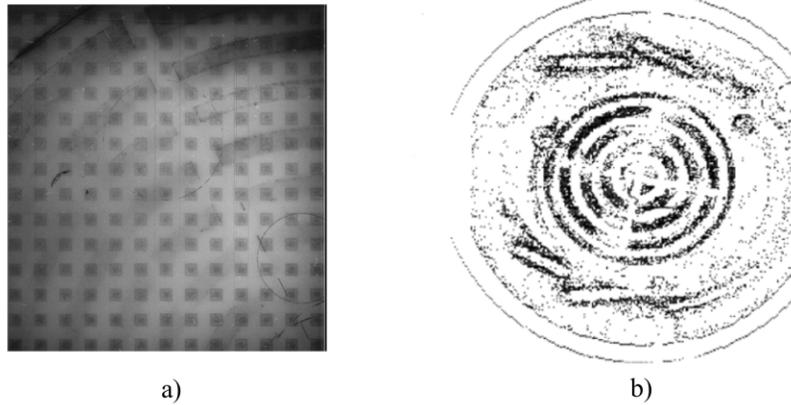


Fig. 2. a) Image taken on a 3512², 10.5 μm pixel CCD operated at -140°C . The CCD was uniformly exposed with 350 nm light generated by illuminating a narrow-band filter with a broad-band source. The periodic, square features correspond to the vacuum chuck used to hold the wafers in place in the photolithography tool. Also visible as concentric rings are patterns from a photoresist dispensing system. b) A particle map of a silicon wafer that was processed with the polished side down through a photoresist dispense system and a photolithography tool.

done the alignment errors are typically smaller than 0.5 μm .

The remainder of the processing includes contact and metal photolithography and etching, alloying of contacts, and deposition of back side anti-reflection coatings by radio-frequency sputtering.

We have found that plasma etching of the contact openings in SiO_2 is one of the more difficult steps in the process. CCDs have large gate electrode areas and are susceptible to plasma damage. We have utilized commercially available plasma monitor wafers to assist in the development of low-damage etch processes [8].

3. Unique fabrication issues for fully depleted, back-illuminated CCDs

Once the ISDP layer is deposited the back surfaces of the wafers will come into contact with automated wafer handling equipment. We have observed that particles and residue from the various vacuum chucks and wafer handlers can imprint patterns onto the back surface of the CCD. Figure 2 a) shows a contrast-enhanced image taken with a 3512², 10.5 μm pixel CCD that was uniformly illuminated at an ultraviolet wavelength of 350 nm. Weak patterns from wafer handling equipment are visible. At this illumination wavelength the absorption depth is small, resulting in a high sensitivity of the CCD quantum efficiency to contamination on

the CCD back surface.

Figure 2 b) shows a particle map generated by exposing the polished side of a silicon test wafer to a photoresist spinner vacuum chuck and to a photolithography aligner tool. The particle map was generated with a KLA-Tencor Model 4500 wafer inspection system that detects particles via scattering of a scanned laser beam. From Fig. 2 b) it is clear that contact of the wafers with wafer handling equipment results in particle deposition on the illumination side of the CCDs, and this in turn can result in artifacts in CCD images as seen in Fig. 2 a).

In order to address this problem we have modified wafer chucks and handlers that contact the back surface of the wafers. This includes the use of wear-resistant Vespel® [9] and other compatible materials in wafer handlers. Silicone in particular is to be avoided as we have found that residues from this material are very difficult to remove from the back surface of the wafers. Mechanical scrubbing of the back sides of the wafers in a liquid solution has been found to be effective at removing particles that arise even when improved materials are used in the tooling.

We have also utilized a sacrificial SiO_2 layer that is deposited on the back side of the wafers after the ISDP step. This technique results in the elimination of direct contact of the ISDP layer with wafer tooling, and allows for efficient pattern removal when the sacrificial layer is chemically removed prior to depo-

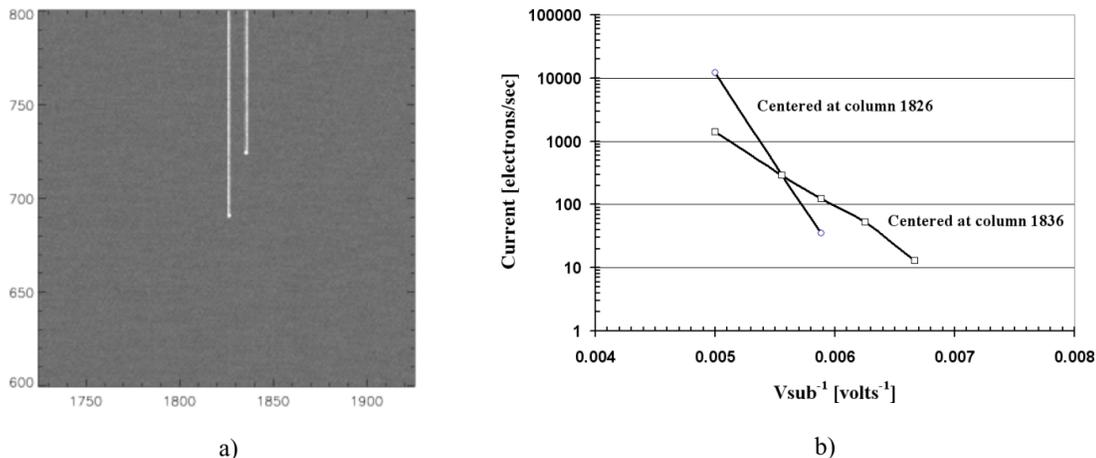


Fig. 3. a) An approximately 290×220 pixel sub-image of a $10.5 \mu\text{m}$ pixel CCD taken under dark conditions at a substrate bias voltage of 180 V and an operating temperature of -140°C . The readout direction is to the bottom. b) Calculated current in electrons/sec versus inverse substrate bias voltage for the two pixels in a) with elevated dark current.

sition of the anti-reflecting coatings. However, since the layer is deposited by radio-frequency sputtering there is ion-bombardment damage to the ISDP layer. This results in an increased etch rate of the damaged portion of the ISDP layer during the SiO_2 removal step, and therefore the starting thickness of the ISDP must be increased to account for this loss.

In addition to the cosmetic defects mentioned above, mechanical damage from wafer handling can lead to high dark current in fully depleted CCDs. In the over-depleted case the electric field at the back side of the wafer can be substantial. Mechanical damage extending beyond the n^+ ISDP layer in Fig. 1 into the depletion region will result in an increase in the dark current. The necessity to make the ISDP layer thin for blue response exacerbates the sensitivity of the CCD dark current to mechanical damage from wafer handling.

Figure 3 shows an example of this. Figure 3 a) shows a sub-image of a $10.5 \mu\text{m}$ CCD operated at a substrate bias of 180 V and an operating temperature of -140°C [6]. Two bright regions of enhanced dark current are observed. The trailing lines of high dark current are generated during the row by row readout of the CCD due to charge injection into those regions during readout. From the measured charge and the known row-shift time, the dark current can be calculated and studied as a function of substrate bias voltage and temperature.

Figure 3 b) shows the calculated dark current versus the inverse substrate bias voltage. The latter is proportional to the electric field at the high-

resistivity silicon- n^+ ISDP interface [4,6]. As can be seen the dark current varies approximately exponentially with electric field. From measurements made at varying temperatures we have also observed that the dark current is an exponential function of temperature, with activation energies in the range of $0.30\text{--}0.36 \text{ eV}$. This behavior is consistent with a trap-assisted tunneling phenomena perhaps including Frenkel-Poole barrier lowering at defects on the back side of the wafer [10,11].

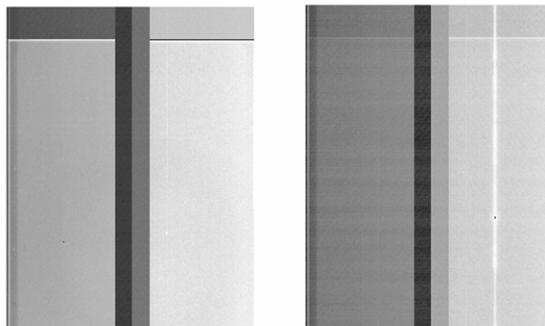
4. CCD screening tests

Once the wafers are fabricated they are initially screened for defects in a probe station. The CCDs are tested at typically -45°C in the dark at nominal voltages followed by separate screening tests at elevated substrate and vertical clock voltages. The latter two tests take advantage of the exponential electric field dependence of dark current for both back side defects as described in the previous section, and for gate insulator flaws [12]. Three images are taken at each test condition, and median filtering is used to remove cosmic ray and background radiation artifacts.

After the automated data taking, analysis software is run on the image files. Figure 4 shows an example printout from the analysis software as well as CCD dark images taken at -45°C on the probe station. The table entries that are not “-1” report CCD columns where the measured charge anywhere in the column exceeds 100 analog to digital units

Column	ADU above Median			% blockage 60s Dark
	Vsub	Parallel	1s Dark	
1033.00	-1.00000	-1.00000	-1.00000	98.4877
1366.00	-1.00000	-1.00000	-1.00000	99.5258
1503.00	202.361	148.858	135.586	-1.00000
1504.00	243.408	160.445	153.816	-1.00000
1531.00	-1.00000	-1.00000	-1.00000	76.2572
1807.00	-1.00000	36597.3	-1.00000	-1.00000
1808.00	-1.00000	46250.1	-1.00000	-1.00000
1809.00	-1.00000	13773.1	-1.00000	-1.00000
2324.00	248.303	211.263	200.207	-1.00000

a)



b)

c)

Fig. 4. a) Printout from the automated wafer probing analysis software for 2048×4096 ($15 \mu\text{m}$ pixel) CCD 114512-21-1. b) Median-filtered dark image taken on CCD 114512-21-1 with a 1 second integration time at -45°C and at nominal operating voltages. c) Median-filtered dark image taken on CCD 114512-21-1 with a 1 second integration at -45°C and at elevated vertical clock voltages.

(ADU) over the mean for the entire CCD. The “1s dark” column denotes testing at nominal voltages, and “Vsub” and “Parallel” report results for elevated substrate and vertical clock levels, respectively. For this particular CCD, a defective region is seen when the vertical clock levels are increased from the nominal values (Fig. 4 c). From the printout it is seen that columns 1807–1809 are affected by this defect. This type of defect is of particular consideration since degradation over time is likely, resulting in long-term reliability concerns [12].

As a result of these efforts we have been able to identify particular steps in the process that can lead to yield loss and are investigating alternative techniques to improve the yield.

5. Summary

We have described fabrication techniques employed at LBNL for the production of fully depleted, back-illuminated CCDs, and have described the unique problems peculiar to the fabrication of this type of device. We have also described CCD screening procedures that are useful in terms of identifying defects and yield loss mechanisms.

6. Acknowledgements

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