Characterization and deployment of large format, fully depleted, back-illuminated, p-channel CCDs for precision astronomy

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ABSTRACT

We present new characterization results for a large format, 15 μm pixel pitch, 2k×4k format, p-channel CCD fabricated on high-resistivity silicon at Lawrence Berkeley National Laboratory. The fully-depleted device is 300 μm thick and backside illuminated utilizing 4-side buttable packaging. We report on measurements of standard operating characteristics including charge transfer efficiency, readout noise, cosmetics performance, dark current, and well depth. We have also made preliminary measurements of the device's X-Ray energy resolution and tests of device linearity.

Keywords: CCD, astronomical imaging, focal plane detectors, SNAP, Lawrence Berkeley National Laboratory

1. Introduction

The modern observational sciences of astronomy and cosmology require unprecedented measurement precision and have created stringent new detector requirements. These requirements include: large, close-packed mosaic arrays; controllable point spread function (PSF) response; single-photon (or single-carrier) sensitivity; low noise detection; intrinsic energy resolution; high quantum efficiency across a broad spectral range; excellent linearity, and more. It is also desired that these requirements be achieved at low cost, are easily implemented, and easily deployed. This paper describes the characterization of an innovative CCD image sensor developed at Lawrence Berkeley National Laboratory (LBNL) aimed at addressing these rigorous new requirements[1].

The LBNL devices are thick (200-300 μm), fully-depleted, back-illuminated devices fabricated on high-resistivity silicon[2,3], and provide extended spectral response[4,5], smaller point-spread function[6,7] and improved radiation tolerance[8,9,10] relative to conventional astronomical-grade CCDs. Features of this CCD include 1) construction on float-zone refined, high-resistivity (5-10 kΩ-cm), n-type silicon, 2) a boron-doped p-type charge transfer channel, 3) an independently applied substrate bias voltage, and 4) fully depleted operation. Figure 1 shows the 3-phase, p-channel CCD design. The 10 kΩ-cm resistivity corresponds to a dopant density in the mid-10^{11} cm^{-3} range, about four orders of magnitude smaller than in conventional CCDs. This permits fully depleted operation at bias voltages of ~20 V – 25 V for 300 μm thick devices. The effect of the bias voltage is to remove mobile electrons from the extremely small number of phosphorous dopant atoms in the silicon creating an electric field, due to the dopant atoms that are now ionized and positively charged. The field extends essentially all the way to the backside contact, depleting the entire volume of the CCD substrate. Figure 2 shows the modeled, 2-dimensional potential field distribution within the silicon.

Fully depleted operation of p-channel devices offers advantages over standard devices. In the p-channel device holes instead of electrons are collected. Also, there are no backside potentials or field-free regions where charge trapping or recombination can occur. Hence, the device thickness is selectable. This allows tailored, high quantum efficiency spectral response (from near-IR to X-Ray) and mechanical behavior. The electric field created by the independently applied substrate bias voltage accelerates photo-generated carriers toward the CCD collection wells resulting in minimal transverse diffusion of carriers, and thus excellent and controllable point spread function response, and also enhanced intrinsic energy resolution. Decoupling the substrate depletion potential and the collection and transfer voltages also allows simplified device optimization.

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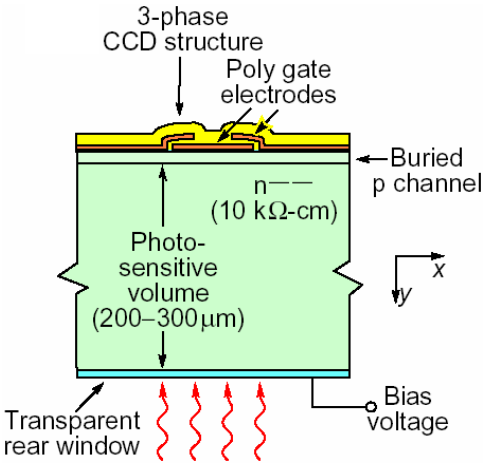

Figure 1. Cross section of the LBNL fully depleted CCD. A conventional buried channel CCD is fabricated on a high-resistivity silicon substrate. A bias voltage applied to the backside electrode results in full depletion.

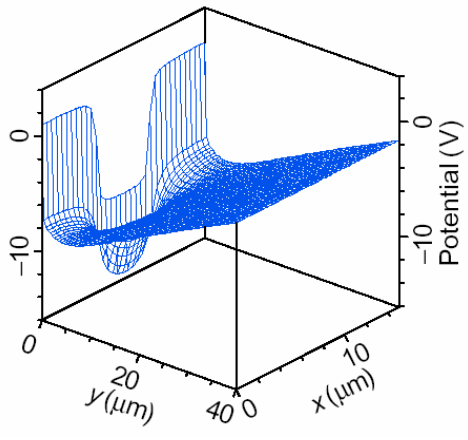

Figure 2. A two-dimensional simulation showing the potential in a fully-depleted LBNL CCD that directs the photo-generated carriers into the traditional potential wells formed by voltages on the frontside CCD gate electrodes.

2. Laboratory Measurements

All CCDs were packaged and tested at the LBNL CCD Production Facility (CPF). The CPF is devoted to developing packaging solutions and providing device characterization for delivery of science grade devices and in support of LBNL on-site fabrication at the Microsystems Laboratory (MSL). The CPF includes a Class 10,000 clean room where "picture frame" and four-side abuttable device packaging is performed. The CPF also has a CCD characterization stand that includes Fe-55 and Cd-109 X-Ray sources, an integrating sphere for flat-field illuminations (~2% uniformity), and an Optiliner projector for flat-field illumination (~5−10% uniformity) and pinhole projections.

2.1 Device Selection and Preparation

Six 15 μm pixel pitch, 2k×4k devices, designed for low-voltage operation ($\leq 40V_{sub}$) and two-corner readout, were selected for packaging and testing. The device schematic is shown in Figure 3. Four of the devices were fabricated at the LBNL Microsystems Laboratory (MSL) and two were fabricated at Dalsa Semiconductor. The shorts yield on the MSL fabricated devices was 100%. All four were ~300 μm thick and potentially science-grade. We obtained images from three of the devices. One of the four was determined to have acceptable cosmetics and was selected for further testing. One of the Dalsa devices was an engineering-grade device with no backside anti-reflection coating and of standard silicon wafer thickness (~ 675 nm). It worked well, had with no shorts and possessed excellent cosmetics; it was used to verify the packaging and characterization protocols. The other Dalsa device was a ~300 μm thick, potentially science-grade device. It was found to have two shorts, which ultimately prevented its operation. Each of the devices was chosen randomly from among several available. None were probed prior to selection for packaging and testing. For future development, an on-wafer cold probing station has been launched at the University of California, Santa Cruz[11]. They will assist LBNL in failure analysis and pre-selection of devices prior to packaging.

The devices were mounted backside-illuminated using a LBNL developed, four-side abuttable package design[12] that utilized a two-side printed aluminum nitride (AlN) substrate supported by a thick molybdenum mount that provided the CCDs' mechanical interface to a cold plate. The AlN provides a good thermal expansion match to silicon and is also a good thermal connector. The device packaging is much simpler than that for standard thinned devices used in astronomy because the thick CCD is mechanically self-supporting. The devices were electrically connected to the AlN substrate by standard aluminum wedge wirebonds. The AlN substrate, in turn, was connected to the control electronics via a 37-pin Nanonics connector soldered to the substrate's surface. The design of the package was determined by specifications for the proposed SuperNova Acceleration Probe Satellite (SNA). The packaging was designed to achieve shim-free integration into a large mosaic while maintaining flatness and co-planarity to less than 10 μm. Figure 4 shows details of the package design. Fully packaged 2k×2k and 2k×4k devices are shown in Figure 5.

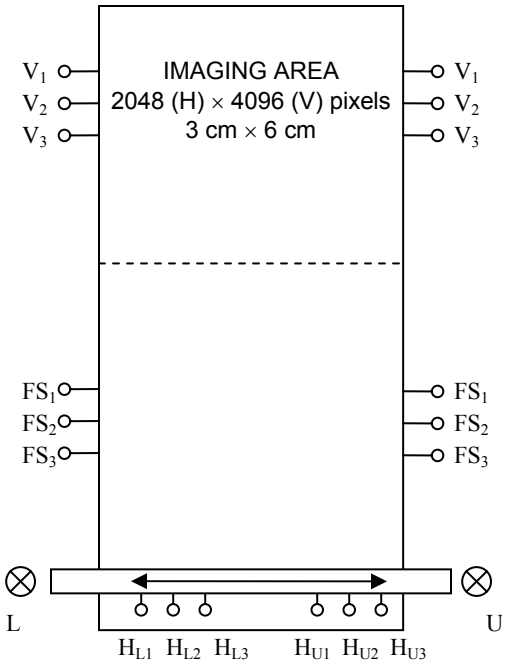

Figure 3. Schematic of the 2048 × 4096-pixel LBNL CCD. V and FS indicate the vertical and framestore parallel clocks. The upper and lower readout stages are labeled U and L respectively. The serial register has independent upper and lower horizontal clock lines.

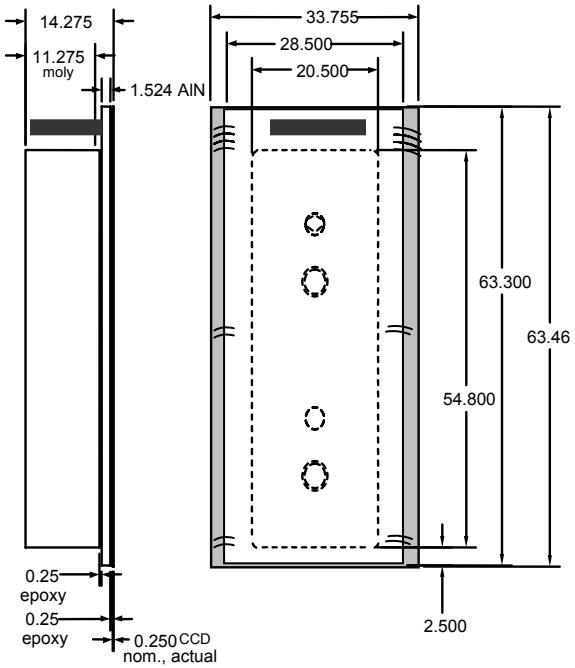

Figure 4. Four-side buttable package design for a 2k×4k device (units in mm). The primary parts of the package are the CCD, a printed AlN substrate, a Moly foot, an electrical connector soldered on the AlN substrate, and wirebonds that connect the CCD to the AlN substrate.

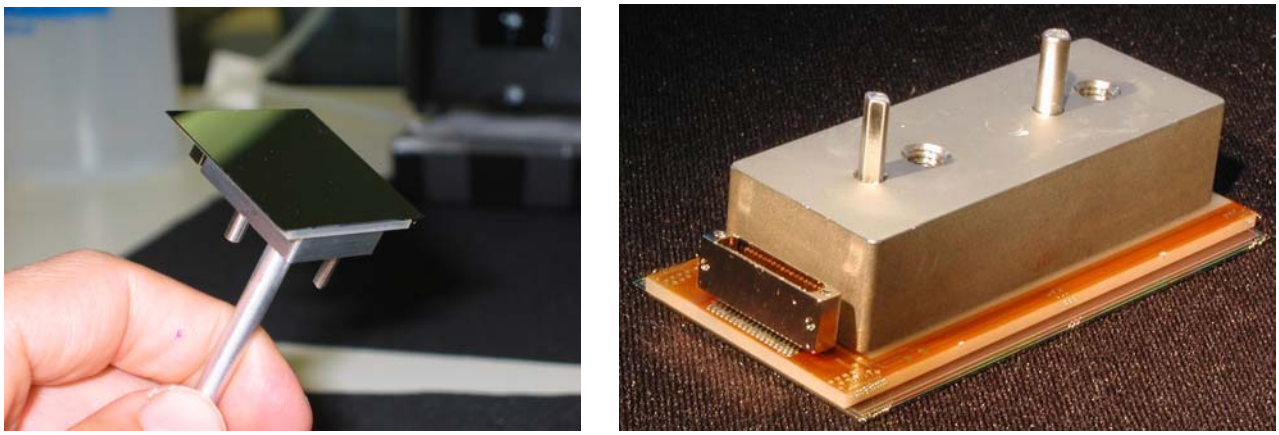

Figure 5. Packaged four-side buttable LBNL 2k×2k and 2k×4k CCDs. Note that the edges of the self-supporting CCDs extend beyond the edges of the AlN substrate. The 300 μm thickness of the high-resistivity device allows a relatively simple four-side abuttable packaging solution utilizing easily implemented wirebonds. The flatness of this design at operating temperature is measured at ≤ ± 2 μm[12]. The packaging solution is also designed to deliver packaged devices with a thickness range of ± 2 μm allowing shim-free integration into large focal plane mosaic arrays.

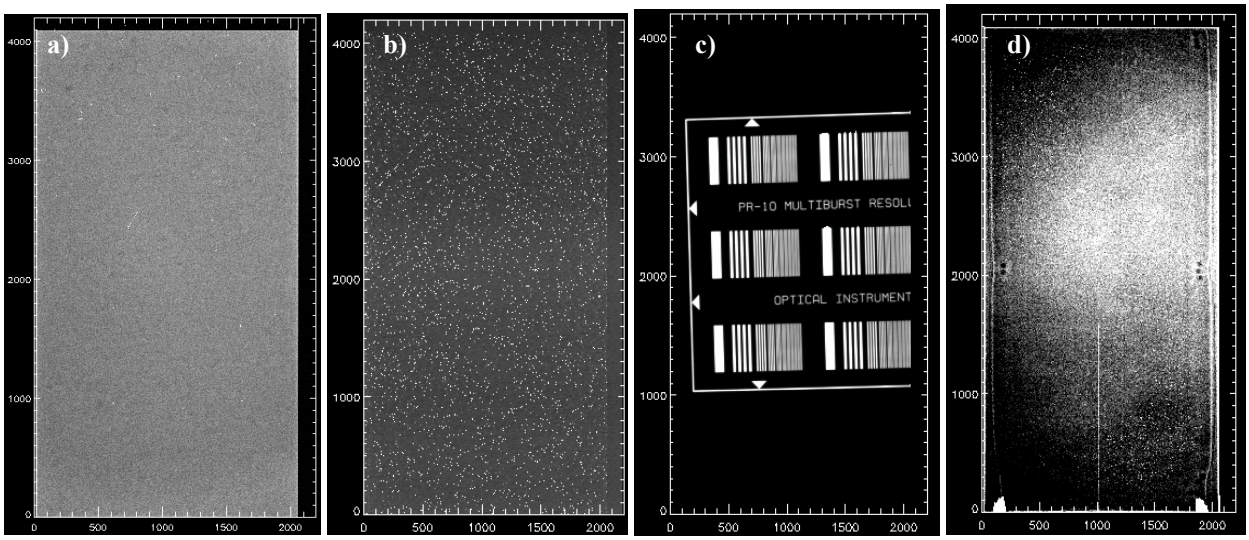

Figure 6. Images taken on the MSL fabricated 2k×4k device selected for further testing: **a)** a bias frame, **b)** Cd-109 X-Ray image, **c)** a resolution bar target image, and **d)** 10,000 e^- level green flat field image (650 ± 21 nm). All images are set to maximum stretch.

2.2 Standard Device Characteristics Measurement

Prior to performing characterization experiments, tests were performed to determine optimal voltage and clocking settings (Table 1). Figure 7 shows the output transfer gate transfer curve. Figure 8 shows the parallel charge transfer efficiency (CTE) as a function of the parallel clock barrier-phase voltage setting. The CTE was measured using the extended pixel edge response (EPER) method at a signal level of ~2,775 e^-. Figures 9 and 10 show the charge transfer clocking schemes. After initial optimization, the readout noise, dark current, and cosmetics were measured using the standard techniques. Table 2 gives the measured device characteristics. The tested device utilized a early transistor gate geometry and performed to specification; current LBNL devices use lower noise, compact geometry transistors, which have reduced readout noise from ~4.5 e^- to ~2 e^-. All of the measured values, after optimization, were to specification.

Table 1. Optimized clocking and bias levels for 2k×4k, low-voltage, high-resistivity CCD

Item	Setting	Item	Setting
Parallel Clock	−2 V and +8 V	Summing Well Clock	-3 and +5
Parallel Clock Overlap	60 µs	Output Gate	5 V
Transfer Gate	−4 V and +8 V	Output Drain	-22 V
Serial Clock	−4 V and +6 V	Reset Drain	-13.5
Serial Clock Rate	32 µs per pixel	Reset Clock	-6 and 0
Substrate Bias	40V	Temperature	-133 C (140 K)

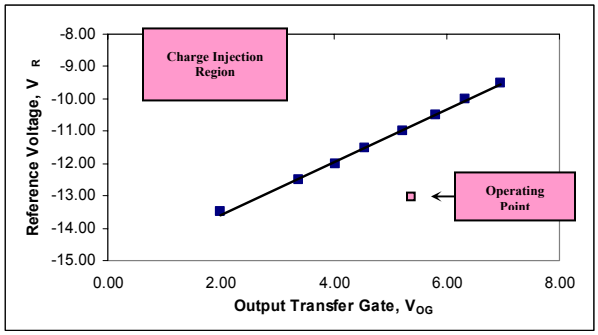

Figure 7. Output transfer gate transfer curve used to determine optimal output gate and reset drain voltages.

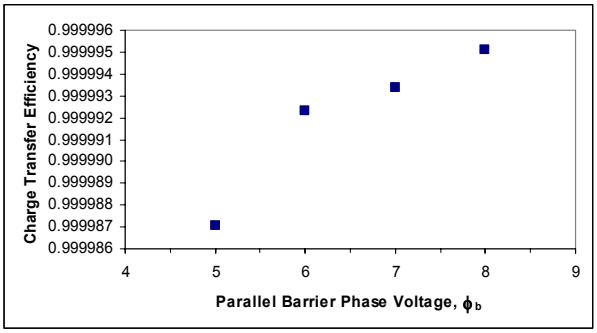

Figure 8. Parallel charge transfer efficiency measured as a function of the barrier voltage via the EPER method.

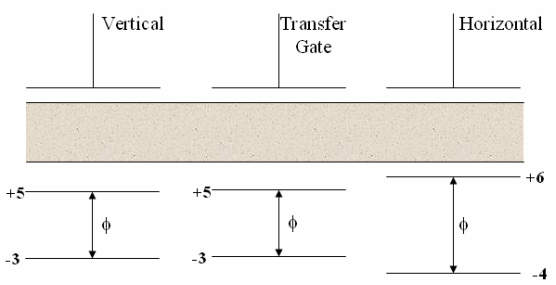

Figure 9. Standard clocking levels for LBNL designed high-resistivity CCDs.

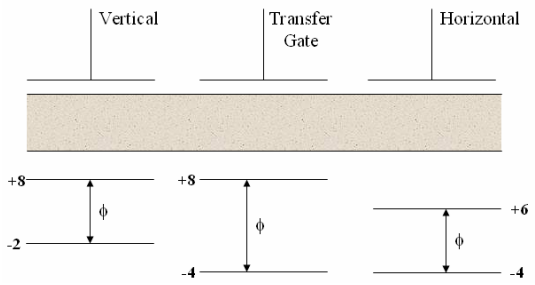

Figure 10. Optimized clocking levels for a MSL-fabricated 2k×4k high-resistivity LBNL CCD.

Table 2. Measured Characteristics of 15 μm pixel pitch, 2k×4k CCD at -133 C

Item	Measured Value
Readout Noise	4.6 e^-
Dark Current	0.002 e^-/pixel/sec
Column Defects	0
White Spots (> 100 e^-/hr)	72
Black Spots (< 80 % mean)	279
Parallel CTE	>0.999995
Serial CTE	>0.999995
Full Well	>250 Ke^-

2.2 Linearity

Precision astronomy and cosmology require low light level sensitivity and measurement uncertainties ≤ 1 – 2 %. The excellent linearity of CCDs facilitates these requirements and allows image subtraction and flatfielding for elimination of backgrounds and instrumental artifacts. In Oluseyi et al. (2004) we described fixed pattern noise features on device images (see Figure 6d) created by residuals from the vias on the AlN substrate that have "printed" through to the CCD. The via residuals are located on the AlN substrate under the CCD's active area near the right and left edges of the device, midway up the CCD. These vias show an average ~ 6% reduction in response from the image median level. An examination of the packaged device revealed that epoxy flowed into and filled the vias near the CCD's edges; there is also a faint bright halo surrounding the depressed circles that correspond to the locations of the vias. On the other hand, vias under the aluminum electrical connector show an enhanced response compared to the local median value. Because of the presence of the connector it is not possible to determine if epoxy flowed into and filled them, though we believe that it is likely the electrical connector would have capped the vias and created an air pocket which would likely prevent epoxy from fully filling them. Also, the presence of the metal connector should provide an optically reflective surface. Note finally that the outside the glue line the edge of the AlN is also apparent. The glue line shows depressed emission of ~ 6% on the interior side and enhanced emission of < 1% on the exterior side. This signal level independent, fixed pattern noise offers additional means of testing the device's linearity and flat-fielding capability: To what degree are the via and glue line residuals removed by standard astronomical flat-fielding? Are there temperature or wavelength dependent effects in the flat-field subtraction? By what mechanism do via and glue line residuals create the observed patterns?

An additional concern for the 300 μm thick device under test, because it is more sensitive to red light than standard CCDs (Figure 10), is its linearity across colors. Short wavelength blue light is absorbed near the device's surface and is more susceptible to surface contaminants than red light, which has a longer absorption length in silicon (Figure 11). If the absorption length of a photon of given wavelength is l, then the fraction of the light absorbed while passing through the silicon CCD of thickness, d, is given by $(1 - e^{-d/l})$. For our 300 μm thick device, the absorption length at 995 nm light is equal the device thickness, 300 μm. Thus, >40% of long wavelength light will pass through the device unabsorbed. Some of this light may reflect off of the CCD/air interface or the CCD/AlN interface, back into the device. We have previously shown evidence that this phenomenon is occurring. Hence, it is necessary to measure the linearity of the device under a range of conditions and at different colors.

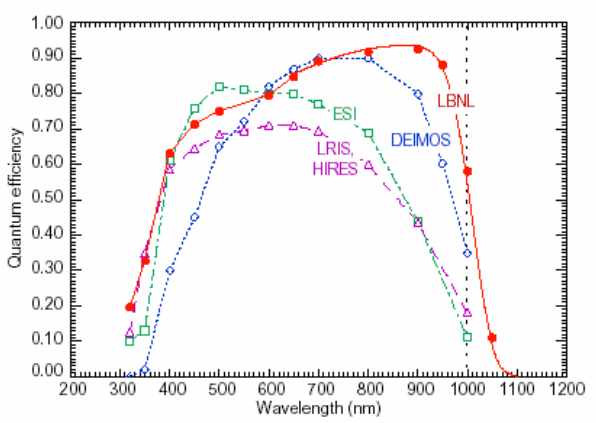

Figure 11. Measured quantum efficiencies comparing a 300 mm thick, fully depleted LBNL CCD versus CCDs in use at the Keck Telescope. The ESI and DEIMOS CCD's were fabricated at MIT Lincoln Laboratory [3], and the HIRES/LRIS CCD's were fabricated at Scientific Imaging Technologies.

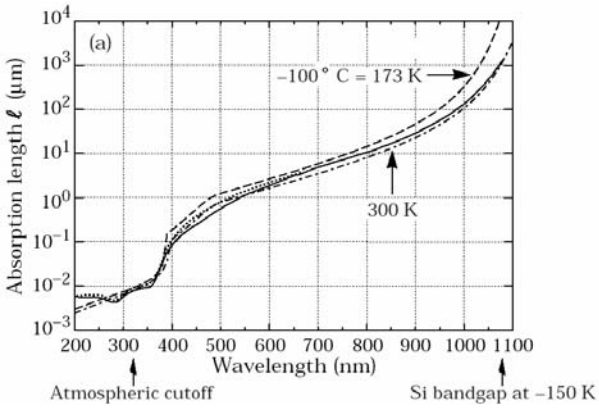

Figure 12. Absorption length of light, *l*, in silicon. Measurements at room temperature (300 K) are shown by the solid curve. [4,5] The dashed curves are calculated from the phenomenological fits by Rajkanan et al. [6]

We have measured the device linearity using the standard linearity transfer curve (Figure 14). Residuals from a least-squares fit to the data are given in Figure 14. Most of the data lie within the ± 0.5 % contours. To further test the device linearity, we obtained a series of 50 low-level images (~100 e^-) taken through a narrowband blue filter (450 ± 12 nm) and repeated through a narrow band red filter (1000 ± 28 nm). A few high-level images (~50,000 e^-) were also taken through each filter. To test the linearity of the devices, the low-level images were summed, a ratio was taken with their respective high-level images (in a particular color), and the resultant ratio images were normalized to their median values. We noted the percentage deviations at various positions on the device. All artifacts were reduced to below the 1% level. This shows excellent linearity and illustrates an absence of an appreciable dark current gradient.

We also tested the flatfielding capability of the device across temperatures and colors. Flat illuminated frames at ≥ 40,000 e^- were obtained in each of two colors (B = 450 nm, R = 1 μm), at two temperatures each (-130 C and -140 C). Average deviations below the median value caused by the vias in each color were: B=-3.84%, R=-8.09%. Ratios taken between images of the same color were able to flatfield to < 0.5%: B/B=0.02%, R/R=0.30%. At the same color but between temperatures via residuals were reduced to: $B/B_{\Delta T}$=0.13%, $R/R_{\Delta T}$=1.52%. Between colors and temperatures the median deviation was: B/R=2.85%, $B/R_{\Delta T.}$=3.49%. The glue line and AlN edge residuals flatfielded to better 0.5% in all cases. Figures 16 shows representative data for flatfielding in a single color at the same and at two different temperatures. Figure 17 shows representative data for flatfielding at two different colors and with two different temperatures. In both figures we see that the 10 K temperature difference impacted flatfielding by about a factor of five. Because of the excellent device linearity, however, the flatfielding was only ~1.5% at the red end of the spectrum.

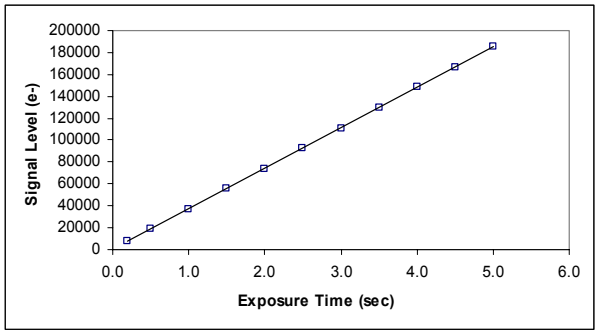

Figure 13. Linearity transfer curve showing the signal versus exposure time for a pinhole illumination.

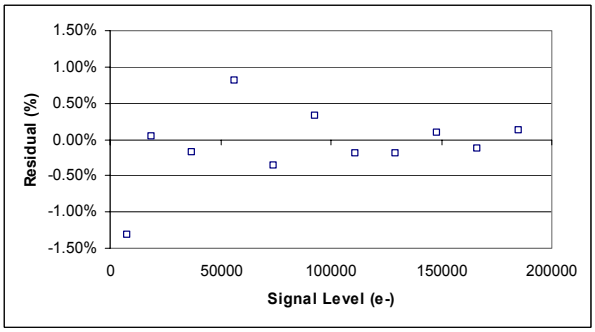

Figure 14. Residual difference of linearity transfer data from a least-squares fit to the measurements.

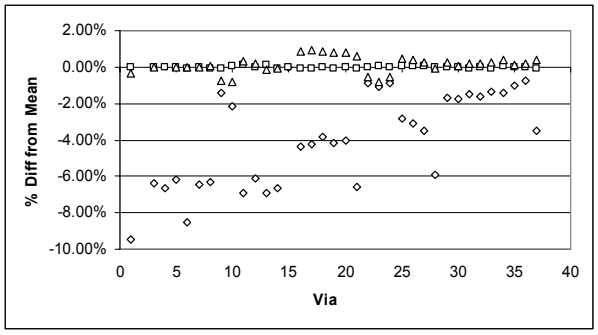

Figure 15. Flatfielding data for one color, blue. The diamonds show the initial levels of the vias prior to flatfielding (see Figures 9 and 10). The squares show the via levels after division of an image through a blue filter by another blue image at the same temperature. The triangles show the levels of the vias after division by a blue image at a different temperature ($\Delta T \sim 10$ K).

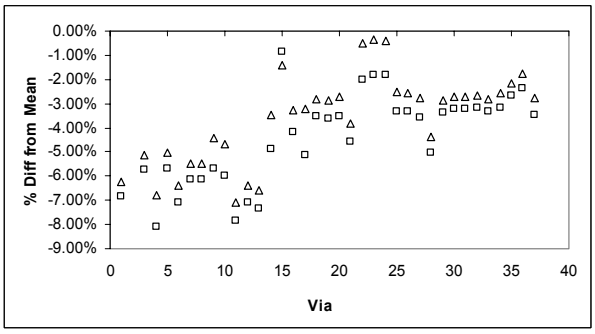

Figure 16. Flatfielding image for two colors. The diamonds show the via residuals after dividing a blue image by a red image, with both images taken at the same temperature. The squares show the via residuals after dividing a blue image by a red image but with the images taken at different temperatures ($\Delta T \sim 10$ K).

2.4 Mean Charge Capture (MCC) and Energy Resolution

A CCD's intrinsic energy resolution derives from the fact that photons of sufficient energy will photo-generate a number of carriers within the CCD that is proportional to the energies of the incident photons. At X-Ray energies, photons become very penetrating. CCD detectors designed for X-Ray detection must, therefore, be thick enough to absorb enough X-Rays to practically serve their purpose. Standard X-Ray CCDs are not operated fully depleted and, thus, suffer loss of charge collection efficiency (CCE). For instance, deep depletion devices only have a depletion depth of 50 μm to 70 μm. The energy resolution of a device to photons of a particular wavelength depends on several factors including the pixel size, the charge collection efficiency, the mean charge capture, and the lateral diffusion within the device. The mean charge capture (MCC) of a CCD is defined as the ratio of charge contained within a target pixel from the absorption of a high-energy photon. The remainder of the charge is contained in the surrounding pixels. The MCC of a device is closely related to the lateral diffusion and pixel size. However, a second-order effect must be considered in the case of the absorption of a high-energy photon. Since photogenerated carriers are produced in a cloud of small dimension, their mutual repulsion, the so-called self-induced drift, can additionally spread photogenerated carriers beyond that caused by lateral diffusion alone. The thick, high-resistivity LBNL devices under test can control the degree of lateral diffusion, and hence the MCC, via the applied bias voltage (Figures 18 & 19).

We have obtained preliminary data on the mean charge capture and energy resolution of the device under test. Note that these results were obtained prior to optimizing the device charge transfer efficiency and thus, can be improved. The CCD was backside illuminated with a Fe-55 (5.9 keV) and a Cd-109 (22 keV) X-Ray source. Source fluxes and distances from the CCD were chosen to provide surface fluences of ~1 photon per ten square pixels. The Fe-55, 5.9 keV photons are absorbed ~30 μm ($1/e$) into the device generating a cloud of ~1620 carriers in a spherical volume of ~0.38 μm. The Cd-109 source should be an excellent tool for measuring the CTE of the back illuminated, 300 μm thick device as the probability for absorption is nearly constant throughout the device, whereas the Fe-55 X-Rays are absorbed very near the backside. ~27% of incident Cd-109, 22 keV photons are absorbed after passing through the 300 μm silicon substrate. The Cd-109 photons generate a cloud of ~6027 carriers in a volume ~3.8 μm. Figure 20 shows a histogram from a Cd-109 illumination giving the energy in single pixels. Figure 21 shows the energy contained in a 3 pixel × 3 pixel square. The positions of the K_α and K_β peaks in the two images indicate that averages of 93% of the carriers generated by the 22 keV photons were captured in a single pixel. The MCC of ~0.93 is an excellent result for the low voltage device ($V_{suv} \leq 40$ V). Note that the current generation of LBNL devices is capable of operating at voltages in excess of 200 V. Also, the lateral diffusion varies as the inverse square root of the applied voltage. Hence, the higher voltage by a factor of five results in an improvement of diffusion control greater than twofold.

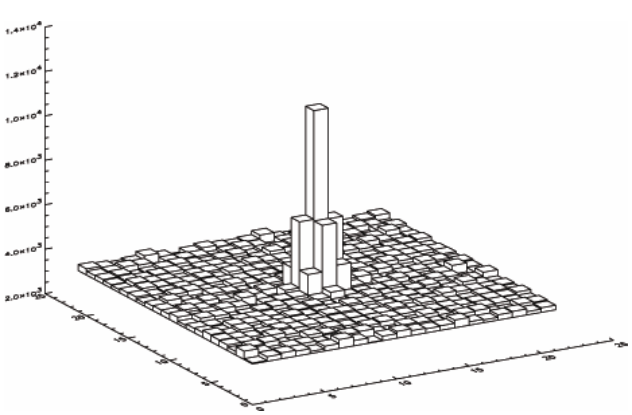

Figure 17. A sub-image from a 300 μm thick, 15 μm pixel pitch, LBNL CCD backside illuminated by an pinhole source with V_{sub} = 20 V.

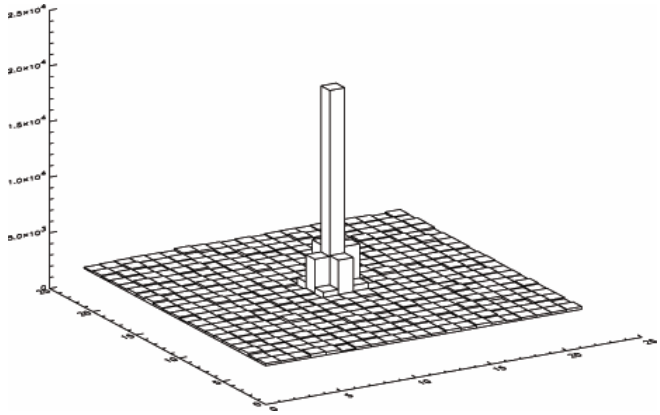

Figure 18. A sub-image from a 300 μm thick, 15 μm pixel pitch, LBNL CCD backside illuminated by a pinhole source with V_{sub} = 60 V.

The source spectrum also provides an indication of the device's energy resolution. The energy resolution, ΔE, expressed as the full width at half-maximum (FWHM) of the device for photons of energy E is determined by the Fano noise, which is the fundamental statistical fluctuation in the photoelectron count, and the device read noise according to Equation 1:

$$\Delta E = 2.354 \times \omega \sqrt{\left(\frac{FE}{\omega}\right) + \sigma_R^2 + other}$$

where F ≅ 0.115 is the Fano factor for silicon;
$\omega \cong 3.68$ eV/e$^-$ is the average energy needed to generate an electron-hole pair at T = -133 C;
σ_R is the read noise of the device, in electrons.

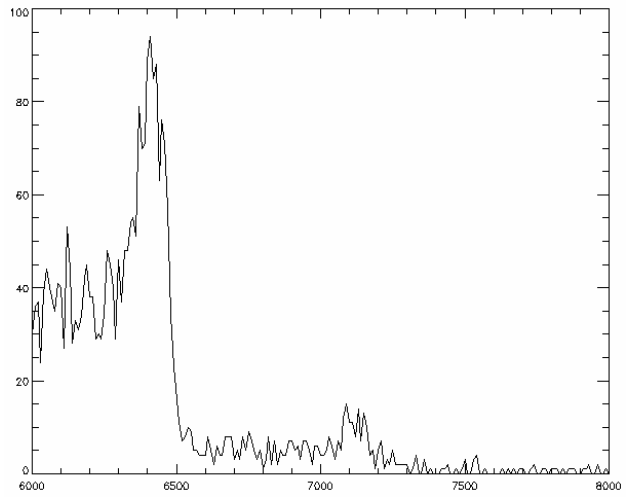

Figure 19. Histogram from an LBNL CCD illuminated with a Cd-109 X-Ray source showing the energy captured in individual pixels. The K_α and K_β peaks occur at 6400 ADU and 7150 ADU respectively.

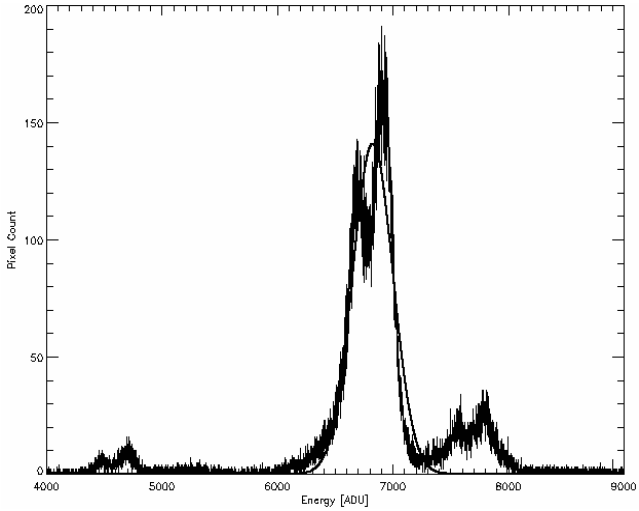

Figure 20. Histogram from an LBNL CCD illuminated with a Cd-109 X-Ray source showing the energy captured in a 3×3 square of pixels. The K_α and K_β peaks occur at 6828 ADU and 7750 ADU respectively.

For the 22 keV Cd-109 K_α X-rays we expect a Fano limited noise of ΔE ~ 231 eV. Utilizing a guassian fit to the 22 keV Cd-109 K_α blend and the measured device gain of 1.14 ADU/e^-, we find widths of ~175 ADU, which corresponds to about 566 eV. The most prominent lines of the Cd-109 K_α blend are K_α at 21.990 keV and $K_{\alpha 2}$ at 22.163 keV. Each is clearly distinguished in Figure 20. Close examination of Figure 20 gives us the FWHM widths of the $K_{\alpha 1}$ and $K_{\alpha 2}$ lines individually. We find widths of σ ~ 90 ADU, which correspond to ~ 291 eV. We note that the results presented here are very preliminary and the data was obtained prior to full device optimization. Hence, the results presented can be improved substantially.

3. Conclusions

We have measured the performance characteristics of a fully depleted, 15 μm pixel pitch, 2k×4k format, p-channel CCD fabricated on high-resistivity, n-type silicon. We have shown that a 4-side buttable packaged, large format, backside-illuminated, 300 μm thick CCD has performed to high specifications. The cosmetics, noise, dark current, full well and charge transfer efficiency were all excellent and consistent with device design specifications.

We have obtained measurements of device linearity using five different methods. 1) the standard linearity transfer curve, 2) the ratio of summed low-level images with a high level image, 3) the ratio of images in the same color taken at different temperatures, 4) the ratio of images at different colors and the same temperature, and 5) the ratio of images in different colors at different temperatures. The device illustrated excellent linearity in all cases. We noted that different types of fixed pattern noise can vary in their degree when the device is illuminated by near-monochromatic light of varying color. Noise created by conditions deep within the substrate or on the side of the device opposite the illuminated side are more dominant in red light, whereas surface pattern noise is more represented in blue light, as expected. The result of this is that flatfielding is somewhat more effective in the blue than in the red.

We have presented preliminary results on the mean charge capture (MCC) and energy resolution of the device under illumination by 22 keV – 25 keV X-Rays. The measured MCC was ~ 0.93. We presented a measured Cd-109 spectrum clearly resolving the $K_{\alpha 1}$, $K_{\alpha 2}$, and K_β lines. Fully depleted operation facilitating the capability to "dial-in" the charge diffusion via the substrate bias voltage and the versatility of selectable device thickness promises improved performance for silicon detectors in the short wavelength regime.

While the performance characteristics measured here are excellent, we note that several upgrades in the newest generation of LBNL high-resistivity devices offer several performance upgrades. Newer devices offer lower readout noise (from 4.6 e^- to 2 e^-), higher voltage operation (from $V_{sub} \leq 40$ V to V_{sub} ~ 200 V), improved 4-side buttable packaging utilizing opaque AlN with no structure under the CCD active area, smaller pixel sizes (15 μm to 10.5 μm), and larger format devices (up to 3.5k × 3.5k)[15].

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