A 2kx2k High Resistivity CCD

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Abstract: We present new results from the characterization of a fully depleted 2048-row and 2048-column (2kx2k) CCD on high resistivity silicon. The CCD was fabricated at the Lawrence Berkeley National Laboratory (LBNL). This device represents a one hundred-fold increase in CCD size compared to devices made previously at LBNL. The large CCD size allows us to do accurate charge transfer efficiency measurements. A two-layer antireflection coating is modelled and compared with laboratory measurements of both quantum efficiency and reflectivity.

Key words: High-resistivity, CCD, quantum efficiency, charge transfer

1. INTRODUCTION

The design and fabrication of small, high resistivity CCDs at the Lawrence Berkeley National Laboratory (LBNL) MicroSystems Lab is described by Holland et.al. [1] and initial test results are described by Stover et.al. [2]. In this earlier work small 200-row by 200-column CCDs were fabricated with 15-μm square pixels. The starting material for these devices is approximately 10,000 Ω-cm float-zone refined n-type silicon, in 300 μm thick wafers.

By application of a bias voltage the entire 300 μm thickness of the CCD can be depleted (all charge within the silicon volume is collected into the pixels), permitting backside illumination without thinning. The 300 μm thickness provides the CCDs with high quantum efficiency in the near-infrared to at least 1 μm wavelength. In addition, thin-film interference fringes, as observed in typical thinned CCDs, are essentially eliminated [3].

Test results from these small CCDs were very encouraging, with high yield and excellent performance. However, the small number of rows and columns limited our ability to accurately measure charge transfer efficiency (CTE), which would become important for larger devices. In addition, these early devices relied entirely on the indium tin oxide (ITO) backside bias contact to provide an antireflection coating. In this paper we present the first test results from a new generation of much larger CCDs. These devices use the same starting material, pixel size, and output amplifier geometry as the earlier generation of CCDs, but the size of the array has been increased to 2048 rows and 2048 columns. In addition, a two-layer antireflection (AR) coating is used to reduce reflections at the silicon surface and thereby improve the quantum efficiency as much as possible. The AR coating is designed to optimize performance at 900 nm wavelength.

2. CHARGE TRANSFER EFFICIENCY

Because the first high resistivity CCDs were only a small array of 200 rows and 200 columns it was difficult to make a precise measurement of CTE. The new devices, with 2048 rows and columns can be used to obtain precise and accurate CTE measurements. These measurements are made by illuminating the CCD with x-rays from Fe^{55}. Each absorbed x-ray creates 1620 signal carriers. (In n-type silicon these are holes). Self repulsion of the resulting charge cloud can lead to significant diffusion which can produce a cloud larger than a single pixel. This effect is minimized by reducing the amount of time required for the charge to collect under the pixel potential wells. X-rays absorbed near the back of the CCD create charge clouds that are as much as 300 μm from the pixels defined at the front side and the time required for the charge to transit to the front side allows for significant diffusion. The easiest way to reduce this transit time is to illuminate the CCD with x-rays from the front side. This assures that a large number of x-rays are absorbed very near the pixel potential wells and a significant number of the x-ray generated charge packets will remain in single pixels.

Figure 1 shows a measurement of parallel CTE using front-side illumination of Fe^{55} x-rays. The cluster of points around 1400 DN represents the charge clouds that are collected within a single pixel. If charge were being lost due to CTE problems the effect would grow as the charge is transferred through more rows, and there would be a slight downward slope to the distribution. As seen in Figure 1 the distribution at 1400 DN shows no slope and the CTE is indistinguishable from 1.0. These measurements were made at a CCD temperature of -130°C and with 50 μs parallel clock overlaps.

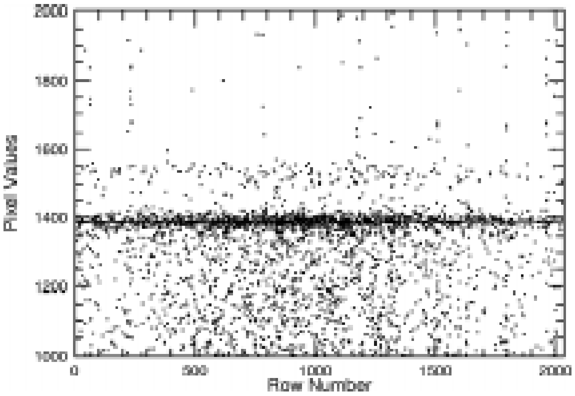

Figure 1. Parallel CTE using Fe^{55} x-rays in front-side illumination.

Figure 2 shows a measurement of serial CTE using front-side illumination. Again the CTE is indistinguishable from 1.0. For these measurements serial clock overlaps were 1 μs. We have run the serial clocks with overlaps as short as 200 ns with no measurable degradation in serial CTE. CCD temperature was -130°C.

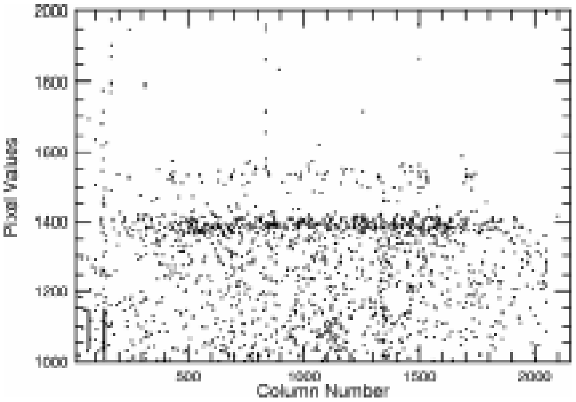

Figure 2. Serial CTE using Fe^{55} x-rays in front-side illumination.

These CTE measurements are very encouraging since it is now clear that much larger CCDs can be produced without CTE concerns and that these CCDs can be clocked at higher speeds without CTE degradation.

3. QUANTUM EFFICIENCY

Quantum efficiency in backside illuminated high resistivity CCDs is controlled by three effects. The first effect is absorption of UV photons (≤400 nm wavelength). These photons are strongly absorbed in the thin (approximately 10-20 nm) polysilicon contact layer on the backside of the CCD. This layer is necessary to help minimize backside dark current. However, the absorption in this layer defines the “blue-side” QE cut-off for these devices.

The second effect which controls QE is the silicon band-gap at just beyond 1100 nm. At this wavelength silicon becomes transparent and QE drops to 0.0 as wavelength increases toward this limit. Nevertheless, because of the 300 μm thickness of the high-resistivity CCDs the QE remains high out to at least 1μm wavelength.

The third effect which controls QE is the reflection of light at the silicon surface. Because of the high index of refraction of silicon (approximately 3.5) reflection losses can be significant and an effective AR coating can greatly improve QE.

Figure 3 is a graph showing both QE and reflectivity for the new generation of high resistivity CCDs. The circles show the measured QE for a two-layer AR-coated, back-side illuminated 2kx2k high resistivity CCD at -130°C. The solid curve is the model prediction [3] which includes silicon absorption including temperature effects, backside polysilicon absorption, and the performance of the AR coating.

The ‘x’ symbols show measured reflectivity (actually 1-reflectivity) from the back side of a silicon wafer AR coated at the same time as the CCD and the dashed curve shows the predicted reflectivity based on the parameters of the AR coating.

Excellent agreement is observed between the AR models and measurements at all wavelengths. The QE model and measurements agree at wavelengths longer than about 500 nm. At shorter wavelengths the measured QE differs from the model apparently because of remaining uncertainty in the details of the absorption in the back-side polysilicon layer. In the thin back-side layer charge diffusion from the polysilicon into the high-resistivity silicon of the CCD seems to play an important role in defining details of the blue-side cut-off. Further modelling of the physics is planned.

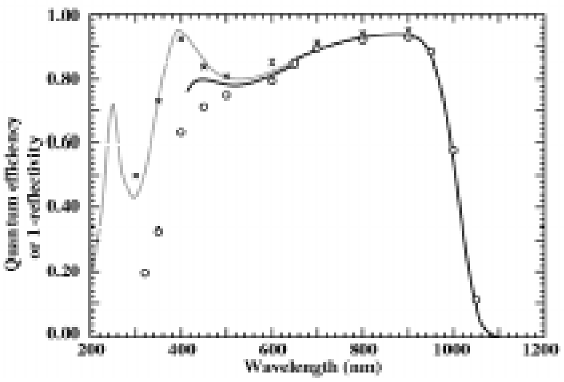

Figure 3. QE

The models predict that the red-side cut-off is slightly temperature dependent and that operation of the CCD at a higher temperature could increase QE at wavelengths greater than 1000 nm.

4. OTHER CHARACTERISTICS

QE uniformity is very good in these devices. At UV wavelengths, where the photons are absorbed close to the silicon surface or in the polysilicon layer, we observed a pattern suggestive of grind and polish marks. The variations in QE which make the pattern visible are less than 1/3 % peak-to-peak. Even this small variation in the UV should be reduced in subsequent devices since an improved polish technique is now used. At wavelengths longer than about 450 nm the QE non-uniformity is much smaller already.

Spurious charge generation can be a significant problem in these CCDs. We have found that wave-shaping of the clocks is necessary to minimize spurious charge.

Amplifier read-noise is 4 to 6 e^- with 8 μs integration times using our double-correlated-sampling amplifier. At 2 μs sampling time the read-noise doubles.

Full well was measured as the level at which the output signal becomes non-linear and was found to be at least 200,000 e^-. Dark current was measured at about 40 e^-/px/hr at -130°C. A technique for surface inversion (similar to MPP operation in some CCDs) is possible but requires some modifications to our CCD controller. We hope to lower the dark current to around 10 e^-/px/hr when these modifications are done.

We have measured the effects of charge diffusion on the point spread function and have compared these results with models. A full discussion of these results is given elsewhere in these proceedings [4].

5. FUTURE PLANS

The next generation of high resistivity CCDs will include a 2kx4k CCD with 15 μm pixels. These devices should become available by the middle of the year 2000. It is currently planned to use one of these CCDs in the ESI spectrograph of the UCO/Keck II telescope.

Longer range developments may include a slightly thinner polysilicon back-side layer to reduce UV photon losses and a multi-layer AR coating that helps to minimize the reflection losses at 300 nm as shown in Figure 3.

Experiments with lower noise on-chip amplifiers are also planned.

6. ACKNOWLEDGEMENTS

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