

Device design for a 12.3 Mpixel, Fully Depleted, Back-Illuminated, High-Voltage Compatible Charge-Coupled Device

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Abstract—A 12.3 Megapixel charge-coupled device (CCD) that can be operated at high substrate bias voltages has been developed in support of a proposal to study dark energy. The pixel size is $10.5\ \mu\text{m}$, and the format is 3512 rows by 3508 columns. The CCD is nominally $200\ \mu\text{m}$ thick and is fabricated on high-resistivity, n-type silicon that allows for fully depleted operation with the application of a substrate bias voltage. The CCD is required to have high quantum efficiency (QE) at near-infrared wavelengths, low noise and dark current, and a spatial resolution of less than $4\ \mu\text{m}$ rms. In order to optimize the spatial resolution and QE, requirements that have conflicting dependencies on the substrate thickness, it is necessary to operate the CCD at large substrate bias voltages. In this work we describe the features of the CCD, summarize the performance, and discuss in detail the device-design techniques used to realize $200\ \mu\text{m}$ thick CCDs that can be operated at substrate bias voltages in excess of 100V.

Index Terms—Charge coupled device, fully depleted, high-resistivity substrate, high voltage, static induction transistor.

I. INTRODUCTION

WE have developed fully depleted, back-illuminated CCDs that address the trade-off of the fully depleted CCD technology in terms of quantum efficiency (QE) and spatial resolution. This work was motivated by a proposal for a space-based telescope to study dark energy [1] – [2].

The substrate thickness in a fully depleted CCD affects both the near-infrared (IR) QE and the spatial resolution [3]. However, these requirements are in conflict in terms of the desired substrate thickness. High near-IR QE requires a thick substrate given the increasing absorption length at long wavelengths in silicon, while the spatial resolution is to first order proportional to device thickness, which demands a thin substrate for good spatial resolution. For a fully depleted p-channel CCD the spatial resolution is determined by the lateral diffusion of the photo-generated holes during their transit from the point of generation to the CCD potential wells [3] – [5]. For a constant electric field the transit time, and therefore the lateral diffusion, decreases with decreasing substrate thickness.

The spatial resolution is also a function of the electric field in the substrate, and the objective of this work was to develop high-voltage capable CCDs that result in good spatial resolution even for the relatively thick substrates that are desired for near-IR response. The main design goal was to allow operation of the CCDs at large substrate bias voltages, on the order of 100V, while still maintaining good performance

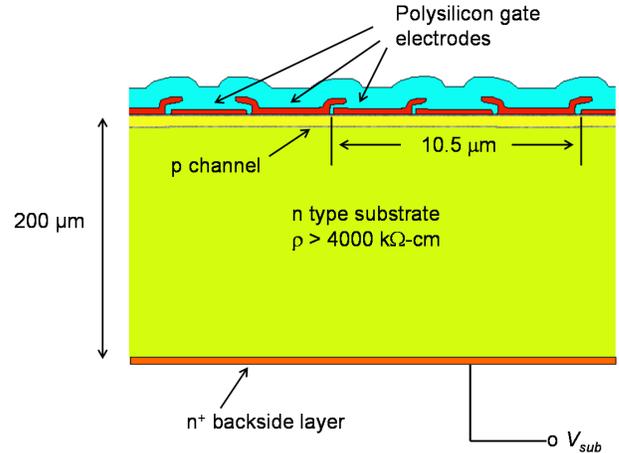


Fig. 1. A simplified cross-sectional drawing of a fully depleted, p-channel CCD. The drawing is not to scale.

in terms of other CCD parameters such as read noise and dark current. The high-voltage compatibility for the CCDs described here is a significant enhancement over the original CCDs developed in our laboratory [3], [6] and more recently under development elsewhere [7] – [10].

The outline of this paper is as follows. The high-voltage compatible (HVC) CCD is described in general terms, followed by a summary of the measured performance. The detailed device design for high-voltage operation is then presented, followed by a discussion of future work.

II. HVC CCD OVERVIEW AND PERFORMANCE RESULTS

A. HVC CCD overview

Figure 1 shows a simplified cross-sectional diagram of a fully depleted CCD. A conventional p-channel CCD structure with 3 layers of polysilicon used to form the 3-phase CCD clocks is fabricated on a high-resistivity, n-type substrate. The CCD is fully depleted by the substrate bias voltage V_{sub} . For simplicity the substrate contact is shown in Fig. 1 making direct contact to the back surface, although in practice this is not feasible given the need for insulating anti-reflection coatings that are deposited on the back surface of the CCD. As a result, in the actual implementation the contact is made on the front side of the CCD [3].

The format is 3512 rows and 3508 columns, the pixel pitch is $10.5\ \mu\text{m}$, and the thickness is $200\ \mu\text{m}$. Figure 2

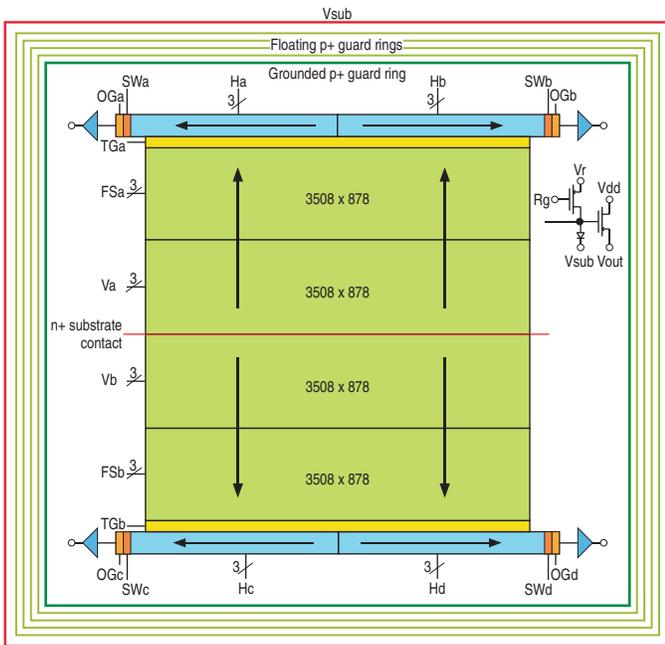


Fig. 2. A block diagram of the HVC CCD. The arrows denote the direction of charge flow. Key: TG: transfer gate, OG: output gate, SW: summing well, H: serial clocks, V: vertical clocks, FS: frame store clocks. The inset circuit diagram shows the detail of the floating diffusion output amplifier.

shows the basic floorplan of the imager. The CCD is a frame-transfer device with 4 readout amplifiers, one at each corner of the device. Conventional floating-diffusion, single-stage source follower amplifiers are used.

An independently clocked transfer gate is used to transfer the charge from the imaging array into the serial registers. The typical voltage excursions for the vertical clocks and the transfer gate are $[+5\text{V}, -3\text{V}]$. The serial registers are clocked to transfer charge in the split mode shown in Fig. 2. The serial clock overlap time is nominally 160 ns, and the clock levels are $[+6\text{V}, -4\text{V}]$.

At the end of each serial register and before the floating diffusion are summing well and output gate structures. The latter is DC-biased, at nominally 2.2V. The summing well can be clocked to allow for the binning of serial charge packets. The serial register itself is wider than the vertical CCD channels in order to accommodate binning. A notch implant is included in the serial registers to confine small-signal charge packets to a narrow, $3\ \mu\text{m}$ wide region. This reduces the number of hole traps encountered during charge shifting [11].

The substrate bias voltage used to fully deplete the CCDs is applied to an implanted n^+ substrate contact ring that surrounds the CCD. A set of four floating p^+ guard rings enclosed by the substrate contact gradually drop the substrate potential to a grounded p^+ guard ring [3] that is in proximity to the CCD imaging area and output amplifier structures. Also, the center of the CCD contains an n^+ substrate contact that runs parallel to the rows. This facilitates the erasure of persistent images from overexposure of the CCD by providing a low-impedance source of electrons that are used between

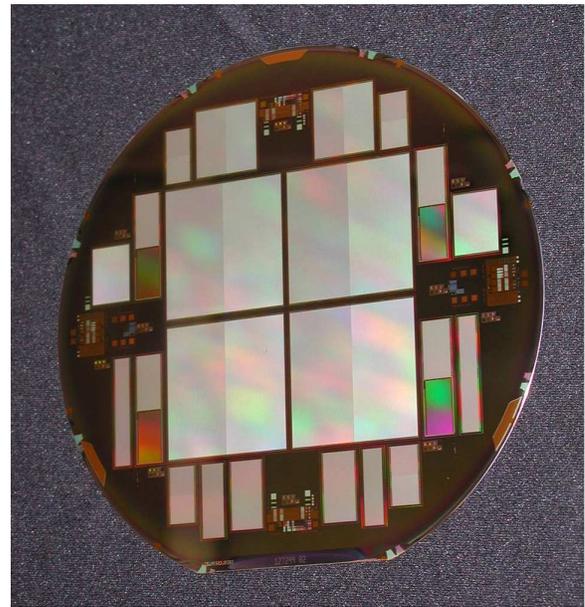


Fig. 3. A photograph of a 150 mm diameter wafer containing 4 HVC CCDs.

frames to recombine with any trapped holes at the silicon-silicon dioxide (SiO_2) interface. This region also prohibits the propagation of saturated columns from bright objects into both halves of the CCD. The width of the n^+ region is equivalent to two rows, although electric field distortions due to the n^+ region cause an effective change in the pixel size for a few rows on either side of the n^+ contact. This is discussed in more detail in Section III-C.

B. HVC CCD fabrication

Figure 3 is a photograph of a 150 mm diameter wafer containing 4 HVC imagers and additional, smaller CCDs. The die size is 38.8 mm (row direction) by 39.4 mm (column direction), and the total imaging area is $13.6\ \text{cm}^2$. The CCD is fabricated in a $2.5\ \mu\text{m}$, triple-polysilicon CCD process with the majority of the processing done at DALSA Semiconductor [12], a commercial foundry. The gate dielectric consists of 50 nm each of SiO_2 and Si_3N_4 .

In order to produce back-illuminated CCDs, wafers from the lot are thinned by a commercial vendor to the final thickness, which for HVC CCDs is typically 200–250 μm . The thinning is done by backgrinding to remove most of the material, followed by fine polishing steps that remove the subsurface damage created by the backgrinding step. The surface finish that results is equivalent to a prime-grade wafer, and the total thickness variation after thinning is typically less than 8 μm .

The fabrication steps required to produce back-illuminated CCDs are then performed at the Lawrence Berkeley National Laboratory (LBNL) MicroSystems Laboratory. A thin, approximately 20–25 nm thick, in-situ doped (phosphorus) polycrystalline silicon layer is deposited on the back side of the thinned wafers by low-pressure chemical vapor deposition at 650°C . This forms the backside n^+ region shown in Fig. 1. Photolithography and etching steps for contact and metal

TABLE I
HVC CCD PERFORMANCE SUMMARY

Parameter	Specification	Result	Notes
QE @ 400 nm (%)	> 50	60	
QE @ 600–950 nm (%)	> 80	> 80	
QE @ 1000 nm (%)	> 50	55	
Read noise (e^- rms)	< 6	3.4 – 4.1	100 kpix/sec
Dark current (e^- /pixel-hour)	< 36	< 5	-140°C
Spatial resolution (μm rms)	< 4	3.7	115V V_{sub}
Linearity (%)	< 1	< 1	At $130 ke^-$
Charge transfer efficiency	> 0.999995	> 0.999995	At $1620 e^-$

definition are then performed on the front side using standard integrated-circuit fabrication equipment. The final steps are the sputter-deposition of anti-reflecting coatings on the backside of the wafer that consist of 55 nm of indium tin oxide and 80 nm of SiO_2 . The CCDs are fabricated using batch-mode processing techniques [13].

C. HVC CCD performance

Table I summarizes the HVC CCD performance goals and reported results [5], [14] – [15]. For scientific applications the CCDs are operated at cryogenic temperatures (-140°C) to reduce dark current, and are read out slowly to minimize the read noise. Correlated double sampling signal processing was used to remove kTC noise and to achieve the 3.4–4.1 e^- read noise. The monochromator-based quantum efficiency setup is described in [16], and the dark current is measured from 30 minute exposures under dark conditions. The spatial resolution measurements have been described previously [4] – [5], and the measured rms diffusion of 3.7 μm at 115V substrate bias is compatible with a pixel size of 10.5 μm . The deviation from linearity of the output response to increasing light levels is less than 1% up to a signal level of 130 ke^- . A radioactive ^{55}Fe source is used to measure the charge transfer efficiency (CTE) [17], and the uncertainty in the CTE measurement is about 5×10^{-7} .

III. HIGH-VOLTAGE COMPATIBLE CCD DEVICE DESIGN

There are several considerations concerning the use of large substrate bias voltages for fully depleted CCDs. Care must be taken to minimize surface potentials that could lead to high electric fields. Avalanche breakdown will result in light emission [18] – [20], and the long-wavelength light emitted in the avalanche process can be detected in the CCD imaging area. Higher levels of impact ionization can lead to excess noise and hot-carrier effects, including charge trapping in insulators that can lead to device failure.

In the following sections we describe 2-D simulations and 1-D analytical calculations used to guide the device design to realize high-voltage compatible CCDs. Before proceeding to that discussion, it is important to note that it is the basic structure of a thick, fully depleted CCD fabricated on high-resistivity silicon that allows one to even contemplate high

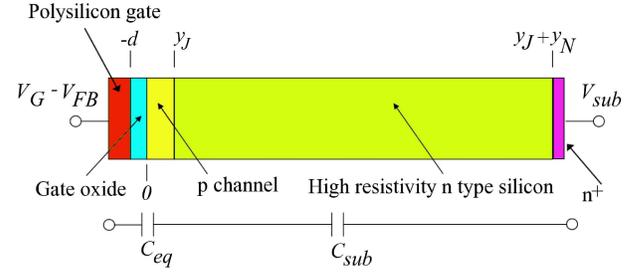


Fig. 4. A simplified cross-sectional drawing of the channel region in a HVC CCD. The drawing is not to scale.

voltage operation. Figure 4 shows a simplified cross-sectional slice through the channel region of the CCD. The buried channel potential minimum occurs in the p-channel, and the charge neutrality condition at the potential minimum location just at full depletion is given by

$$\frac{qN_A}{\epsilon_{\text{Si}}}(y_J - y_{\min}) = \frac{qN_D}{\epsilon_{\text{Si}}}y_N \quad (1)$$

where q is the electron charge, N_A and N_D are the doping densities in the p-channel and substrate, respectively, y_J and y_{\min} are the locations of the p-n junction and CCD potential minimum, respectively, y_N is the thickness of the high-resistivity region, and ϵ_{Si} is the permittivity of silicon. At y_{\min} the electric field is zero and is of opposite sign on each side of y_{\min} , resulting in a potential minimum. The term on the left is the fraction of ionized acceptors in the fully depleted p-channel whose field lines terminate on ionized donors in the fully depleted substrate. Solving for y_{\min} yields

$$y_{\min} = \frac{1}{N_A}(N_A y_J - N_D y_N) \quad (2)$$

Typical values for the channel parameters in Eq. 2 are a few 10^{16} cm^{-3} for N_A and about 1 μm for y_J . N_D for 4 $k\Omega\text{-cm}$ n-type silicon is $1.1 \times 10^{12} \text{ cm}^{-3}$, and for y_N equal to 200 μm it is seen that $N_A y_J$ is about 100 times larger than $N_D y_N$. Therefore $y_{\min} \approx y_J$, and nearly all the field lines in the fully depleted p-channel terminate on the gate electrode. The effect of increasing the substrate bias voltage is to only slightly increase the percentage of field lines from the p-channel that terminate in the substrate, with most of the additional bias voltage being dropped across the high-resistivity substrate.

Quantitatively, a 1-D analytical solution to the Poisson equation for V_{sub} exceeding the depletion voltage yields the following approximate expression for the potential V_J at the p-channel/n-substrate junction of

$$V_J \approx V_G - V_{FB} - \frac{qN_A}{2\epsilon_{\text{Si}}}y_J^2 \left(1 + \frac{2\epsilon_{\text{Si}}d}{\epsilon_{\text{SiO}_2}y_J} \right). \quad (3)$$

where V_G is the applied gate voltage, V_{FB} is the flat-band voltage, d is the gate insulator thickness, and ϵ_{SiO_2} is the permittivity of silicon dioxide [3]. The approximation given in Eq. 3 is valid for $N_D \ll N_A$ and $y_N \gg y_J + (\epsilon_{\text{Si}}/\epsilon_{\text{SiO}_2})d$. From the discussion above V_J is approximately equal to V_{\min} , the CCD potential minimum, and the potential minimum is approximately independent of the substrate bias voltage. The relative insensitivity of the CCD potential minimum to the

substrate bias voltage is key to the ability to operate fully depleted CCDs at large V_{sub} .

The inequality $y_N \gg y_J + (\epsilon_{Si}/\epsilon_{SiO_2})d$ can be rewritten as $C_{eq} \gg C_{sub}$, where C_{sub} is ϵ_{Si}/y_N and C_{eq} is the series combination of the p-channel and gate dielectric capacitances, i.e.

$$\frac{1}{C_{eq}} = \frac{y_J}{\epsilon_{Si}} + \frac{d}{\epsilon_{SiO_2}}. \quad (4)$$

The equivalent circuit consisting of these small signal capacitors is also shown in Fig. 4, and from the circuit it is clear that the potential at the pn junction, which is approximately the potential minimum, is a weak function of V_{sub} due to the capacitor voltage divider formed from C_{eq} and C_{sub} .

In the following sections we describe the device design methods used to reduce surface potentials near the output transistor and in the channel stop regions, and how these issues affect the layout of the CCD. Experimental results are compared to the 2-D simulations and 1-D analytical calculations, and techniques used in the HVC CCD to reduce surface electric fields are discussed. The problem of electric field distortions near the edge of the imaging array resulting in poorly defined pixel volumes is also investigated via simulation.

A. Mitigation of high surface potentials due to parasitic static induction transistors

Figure 5 shows a simplified cross section that illustrates some of the challenges to reducing surface potentials in fully depleted CCDs. Shown in Fig. 5 is the substrate connection where the substrate bias voltage is applied, portions of the floating and grounded p⁺ junctions used to gradually reduce the surface potential from V_{sub} to ground [3], an n⁺ substrate contact, and a buried channel transistor of the type used in the CCD output amplifier. The use of floating guard rings is a standard technique developed for power semiconductor devices in order to achieve high breakdown voltages [21] – [23], and this arrangement provides low potentials on the side of the grounded p⁺ junction that faces the floating junctions. The 2-D device simulator SYNOPSIS Medici was used to design the guard ring structure as well as for the simulations that follow.

The region between the grounded p⁺ junction and the output transistor requires special consideration. The spacing x_p between the grounded junction and the nearest p⁺ electrode of the output transistor is an important parameter with regards to surface potentials. In the previous fully depleted CCDs developed in our laboratory this spacing was very large, resulting in an undepleted region between the biased p⁺ junctions. Since the backside of the CCD is an equipotential biased at V_{sub} , the surface potential in the region between the grounded junction and the output transistor is also equal to V_{sub} . This was tolerable for substrate bias voltages in the 20–40V range. The undepleted region functioned adequately as an ac ground for the output amplifier, and we empirically observed that some but not all CCDs could withstand bias voltages exceeding 100V. However, it was felt that having such high potentials near the output amplifier and imaging

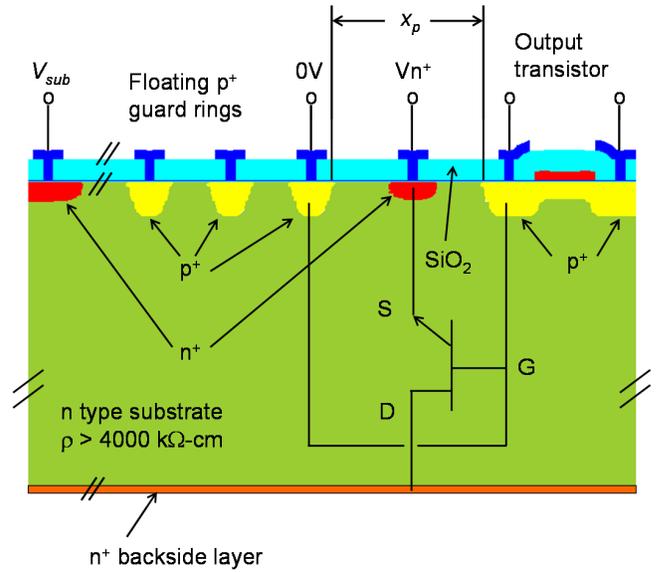


Fig. 5. Cross sectional diagram of the region near an output transistor in the HVC CCD. The drawing is not to scale. S, G, and D refer to the parasitic static induction transistor source, gate, and drain electrodes, respectively.

arrays was not a viable solution to the problem of high-voltage operation.

The remedy chosen was to reduce the spacing x_p and to bias the local substrate connection labeled V_{n+} in Fig. 5 in such a way as to not allow an electron current to flow between the V_{n+} electrode and the backside contact where the potential is V_{sub} [24]. As described later, this biasing is accomplished with an external large value resistor and bypass capacitor.

When x_p is reduced to the point where the depletion regions from the grounded p⁺ guard ring and output transistor merge, one no longer has an ohmic path through undepleted silicon to the backside layer. However, electron injection into the substrate from the n⁺ contact via thermionic emission is still possible. When the depletion regions merge beneath the n⁺ contact a parasitic static induction transistor (SIT) [7], [25] is formed with the topside n⁺ contact the SIT source, the adjacent p⁺ regions the gate electrodes, and the backside layer the drain. The parasitic SIT is shown schematically in Fig. 5.

The drain current in a SIT is increased by barrier height lowering via the gate to source and drain to source potentials. The dependence of the SIT barrier height on geometry and doping does not lend itself to simple analytical modeling given the 2-D nature of the problem. As a result we have used simulation to study the dependence of the SIT turn-on behavior on the spacing x_p , substrate thickness y_N , and substrate bias voltage V_{sub} . Figure 6 shows a 2-D cross section used to simulate the parasitic SIT. Some of the features shown in Fig. 6 relate to junction termination techniques that are discussed in more detail in Section III-C. Fig. 6 shows the equipotential lines at $V_{sub} = 100V$ with the n⁺ contact biased with a current source. One can see the characteristic saddle-shaped SIT potential barrier [26].

Figure 7 shows the simulated floating potential V_{n+} versus the substrate bias voltage for x_p values of 50, 30, and

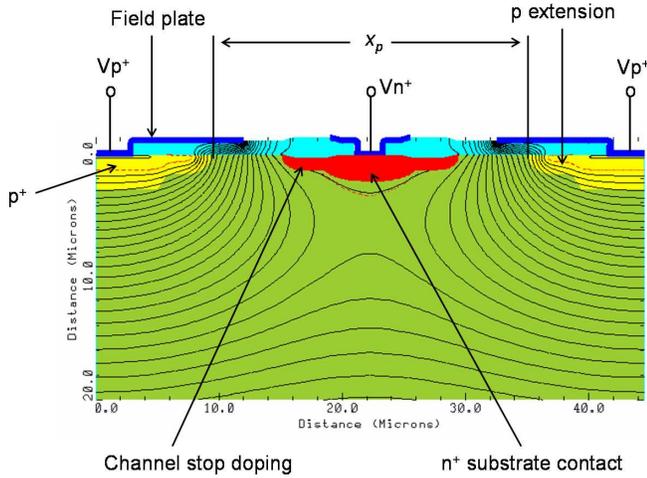


Fig. 6. Simulation cross section for a parasitic SIT. Both p^+ junctions were grounded, and the n^+ substrate contact was biased with a -1 pA current source. The substrate bias voltage was 100V, and the equipotential lines are spaced 0.8V apart.

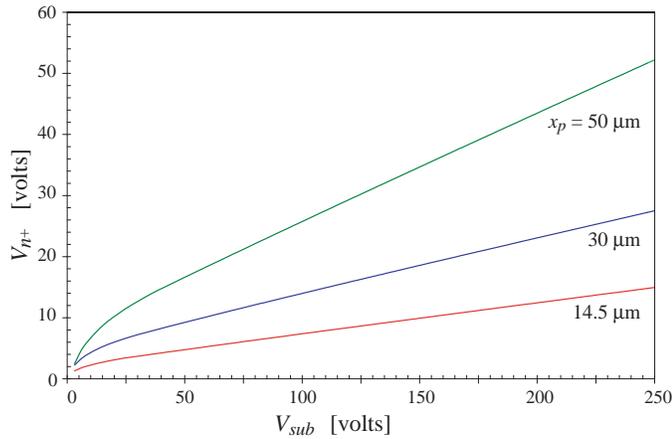


Fig. 7. Simulated potentials at the n^+ contact of Fig. 5 as a function of the substrate bias voltage for various p^+ - p^+ spacings x_p . The potential is that resulting from a current source bias of the n^+ contact of Fig. 6. For the simulation one p^+ junction was grounded, and the other was biased at -22 V. The simulated substrate thickness was 200 μm and the temperature was -140°C .

14.5 μm . The floating potential is simulated by biasing the V_{n^+} electrode in Fig. 6 with a -1 pA current source. The floating potential is a useful parameter in that it models the turn-on voltage of the SIT, and therefore sets a lower limit on the bias voltage required to maintain the SIT in a non-conducting state. As shown below, it is also possible to measure floating potentials on the fully depleted CCDs and compare the simulations to experimental results. From the simulations shown in Fig. 7 it is clear that reducing x_p is beneficial in terms of reducing the surface potentials due to the parasitic SIT, and that potentials substantially less than V_{sub} are predicted for sufficiently small x_p . From other simulations we observe that the floating potentials at a given V_{sub} value are increased as the substrate thickness is decreased. A thinner substrate results in a higher vertical electric field. This reduces

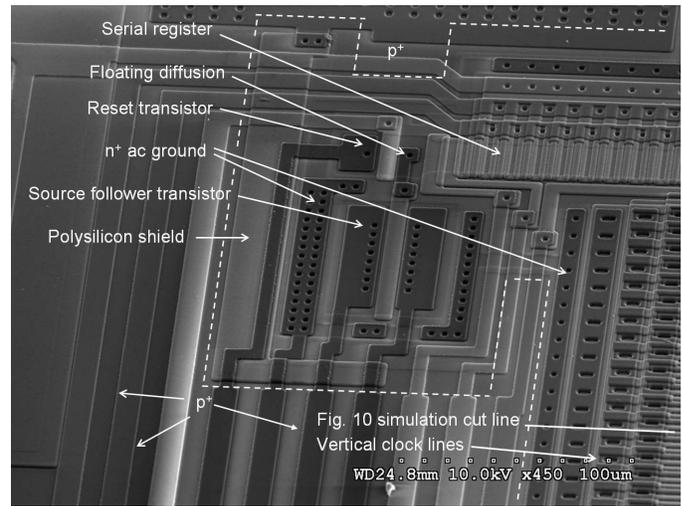


Fig. 8. Scanning electron micrograph showing the output transistor region of a HVC CCD. Regions outside the dashed lines are doped p^+ in an attempt to surround the output transistor region in order to approximate the situation shown in Fig. 6. The simulation cut line corresponding to Fig. 10 is shown in the lower right portion of the figure. Fig. 2 shows the electrical schematic corresponding to the floating diffusion and transistors shown above.

the barrier height, resulting in a higher floating potential representing the onset of conduction of the SIT.

Figure 6 is, however, a simplified representation of the actual device that is shown in Fig. 8. This figure shows a scanning electron micrograph of the output transistor region of the HVC CCD. The source follower transistor is surrounded by a biased n^+ region that acts as an ac ground, and as much as possible there are p^+ doped regions near the transistor in order to reduce surface potentials as per the discussion above. Parasitic SIT's are present between the transistor p^+ source/drain regions and the "sea" of p^+ surrounding the transistor. In some cases the nearest depletion regions come from p-channel regions, i.e. the serial register. Despite the complexity of the actual device we have found that 2-D simulations through various cut lines of Fig. 8 give qualitatively similar results to what is measured, and that the simulation effort was very useful in guiding the design.

Figure 9 shows experimental measurements of the floating potentials on HVC CCDs. The n^+ substrate contact surrounding the transistor in Fig. 8 is routed entirely around the CCD vertical and serial registers, and is brought out to bonding pads that allow direct measurement of the potential. For most of the measurements the n^+ region was floating, and the potential was measured with a high-impedance electrometer. For the curves labeled "3 M Ω " the external connection was biased with a large bypass capacitor and 3 M Ω resistor. In actual operation of the CCD it is necessary that the n^+ region be an ac ground, and this biasing arrangement has been found to work well. The 3 M Ω resistor typically limits the parasitic SIT current to a few μA .

Essentially three classes of CCDs are shown in Fig. 9. The upper curves are for an earlier prototype version of the HVC CCD with a worst-case p^+ - p^+ spacing x_p of about

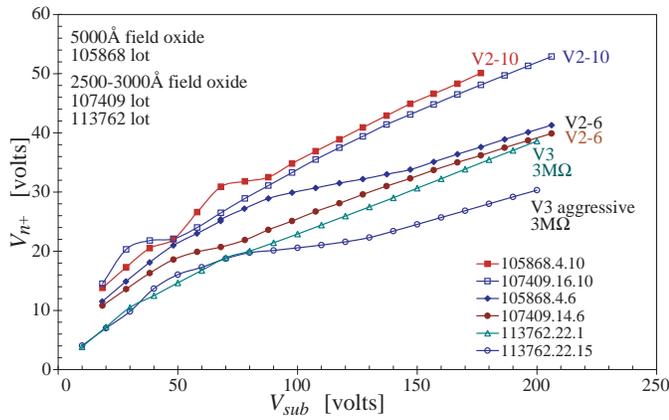


Fig. 9. Measured floating potentials V_{n^+} versus the substrate bias voltage for various versions of the HVC CCD. The potential was measured with a high-impedance electrometer. Two different field-oxide thickness values of approximately 500 and 250 nm were used in the CCD fabrication.

80 μm . The second set of curves with V_{n^+} values of about 40V at $V_{sub} = 200V$ have a spacing of about 50–65 μm , with the former being the value used in the final version of the HVC CCD. Finally, the spacing for the curve labeled “V3 aggressive” was about 35 μm . This was measured on a 1700×1836 version of the HVC CCD with more aggressive p^+ - p^+ spacings than used in the 12.3 Megapixel CCD. Fig. 9 shows qualitative agreement with the simulations shown in Fig. 7, and in particular shows a significant reduction in the measured surface potentials as the p^+ - p^+ spacing is reduced. The final version of the HVC CCD has a measured surface potential of about 22V at a substrate bias voltage of 100V, and we have reported operation of HVC CCDs at substrate bias voltages as large as 200V [5], [24].

B. Study of surface potentials from the channel stop regions

One additional structural feature that was varied in the CCDs reported in Fig. 9 was the field oxide thickness. The field oxide is the oxide layer over the channel stop implanted region (see Fig. 6). This parameter also affects the surface potentials as shown below.

Figure 10 shows a cross-section where metal contact to the three polysilicon vertical clock lines is made. The polysilicon lines extend into the imaging array on the right side of the diagram. This region is also shown as a simulation cut line in Fig. 8. For large format CCDs it is necessary to supply large currents to charge the substantial capacitance of the polysilicon lines, and the metal contacting the polysilicon must be sufficiently wide to avoid electromigration failure due to high current densities in the metal. This results in a large spacing between the grounded p^+ guard ring and the p-channel implants in the imaging area.

Also shown in Fig. 10 is the channel stop region containing the n-type channel stop implant under the field oxide. For large implant doses the channel stop implanted region will not be fully depleted, and the result will be a parasitic SIT with a wide source region that will require high voltages on the nearby n^+

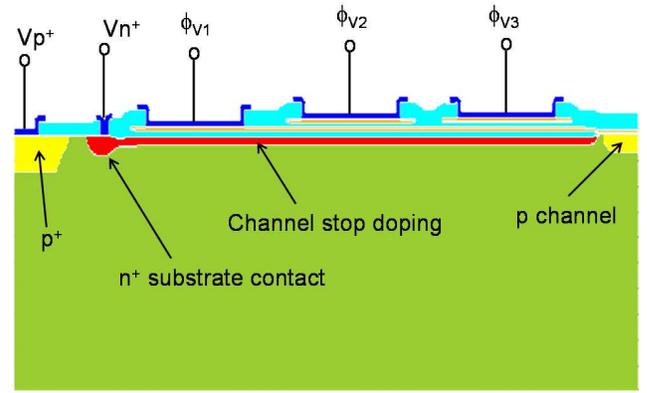


Fig. 10. Simulation cross section of the region where metal contact to the vertical clocks is made corresponding to the simulation cut line shown in Fig. 8. ϕ_{V1} , ϕ_{V2} , and ϕ_{V3} are the vertical clock signals.

contact to maintain the SIT in the off state. For the structure shown in Fig. 10 the gate electrodes of the SIT are formed by the p^+ and p-channel regions, and the SIT drain is as before the backside substrate contact. One could also consider a low-dose channel stop implant that would result in a fully depleted channel stop. It is shown in the Appendix that the potential at the channel stop-field oxide interface from a 1-D solution to the Poisson equation assuming both the channel stop and substrate are fully depleted is

$$V_{\text{surface}} = V_G - V_{FB} - E_{ox} d_{cs} \quad (5)$$

where V_G is the voltage applied to the polysilicon gate that is over the channel stop region, d_{cs} is the thickness of the field oxide, and E_{ox} is the electric field in the field oxide. The cross section for this calculation is nearly the same as the channel cross-section of Fig. 4 but with the doping of the p-channel region changed to n-type.

Similarly to the case of the p-channel, the surface potential under the channel stop is approximately independent of V_{sub} when the substrate thickness is much larger than the channel stop thickness and the doping level in the channel stop is much larger than that in the substrate. When these conditions are met it is shown in the Appendix that the surface potential is

$$V_{\text{surface}} \approx V_G - V_{FB} + \frac{q N_{D,cs} y_{cs}}{C_{ox,cs}}, \quad (6)$$

where $N_{D,cs}$ is the doping level in the channel stop, y_{cs} is the thickness of the channel stop, and $C_{ox,cs} = \epsilon_{SiO_2}/d_{cs}$ is the field-oxide capacitance per unit area. The interpretation of Eq. 6 is as follows. The electric field at the silicon-field oxide interface is dominated by the ionized donors in the channel stop since $N_{D,cs} y_{cs} \gg N_D y_N$, where as before N_D and y_N are the doping in the substrate and the substrate thickness, respectively. An increase in the substrate bias voltage increases the ionized donor density in the backside n^+ contact by a small amount relative to the space charge from the channel-stop implant, and hence the surface potential is a weak function of V_{sub} for a thick, fully depleted CCD fabricated on high-resistivity silicon. According to Eq. 6, one can lower the

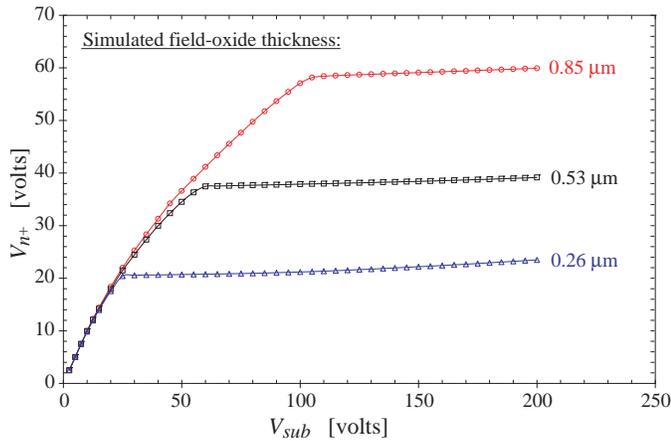


Fig. 11. Simulated floating potentials measured at the V_{n^+} contact versus V_{sub} for the cross section shown in Fig. 10. The n^+ contact was biased with a -1 pA current source to simulate the floating condition. The fixed oxide charge density was $3 \times 10^{11} \text{ cm}^{-2}$.

surface potential by reducing the channel stop doping and thickness as well as the field-oxide thickness. The channel stop thickness cannot be affected significantly given that it is determined by the diffusion of ion-implanted dopants, but the channel stop doping and field-oxide thickness can be varied to lower surface potentials.

Figure 11 shows simulated floating potentials using the cross-section of the vertical clock region shown in Fig. 10. Floating potentials are shown for three oxide thickness values extracted from the SYNOPSIS TSUPREM4 simulation (0.85, 0.53 and $0.26 \mu\text{m}$). The fixed oxide charge density was varied in the Medici simulation with Fig. 11 showing the results for $N_F = 3 \times 10^{11} \text{ cm}^{-2}$. The oxide charge adds a term to the flatband voltage of $qN_F/C_{ox,cs}$. As predicted by Eq. 6 the floating potential is nearly constant once the channel stop is fully depleted, and the saturation value of the potential scales with field-oxide thickness. Saturation values calculated from the simple 1-D model of Eq. 6 for N_F values of 1 and $3 \times 10^{11} \text{ cm}^{-2}$ agree with the 2-D simulation results to within about 20% in the worst case.

Figure 12 compares the simulation results to experimental data taken on early generation HVC CCDs. The results shown are from CCDs fabricated in the same processing lot but with different field-oxide thickness values. The nominal field-oxide thickness was about $0.9 \mu\text{m}$, and about $0.5 \mu\text{m}$ for half the wafers in the lot. Results are also shown for 200 and $650 \mu\text{m}$ thick CCDs. The n^+ potential was measured with a high-impedance electrometer connected to the n^+ substrate contact in the center of the imaging array that was described in Section II-A. This electrode is connected to the wide channel stop region of Fig. 10 via the channel stop implant. The measured potentials are roughly similar to those expected from the simulations and Eq. 6, at least in terms of the saturation value of the potential. In order to reduce the potential from the fully depleted channel stops we are using a 250–300 nm thick field oxide in the HVC CCDs.

In the version of the HVC CCD reported in Fig. 12 there were no n^+ substrate contacts near the output transistors, and

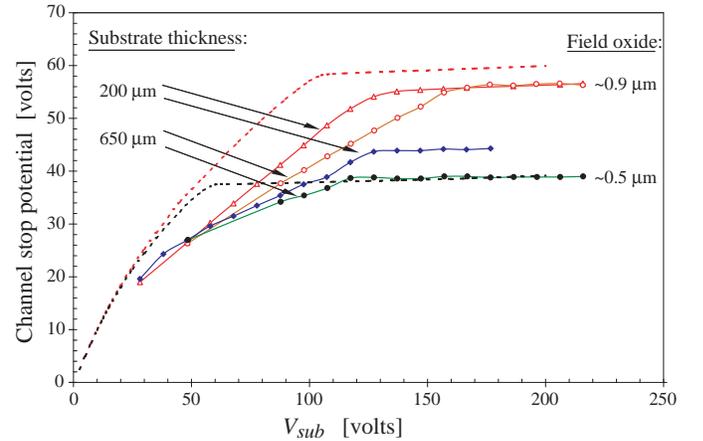


Fig. 12. Simulated floating potentials from Fig. 11 versus the measured n^+ potential on CCDs fabricated in the same lot but with different field-oxide and substrate thickness values. The dashed lines are the simulation results.

we believe this is why we see little if any evidence of the floating potentials expected for parasitic SITs near the output transistor as shown in Fig. 9. We observed in this generation of CCDs that the channel stop region surrounding the transistors was not in thermal equilibrium due to a large impedance between the channel stop and the n^+ electrode connection that was located in the center of the die. We speculated that the high impedance resulted in the inability of the channel stop doping levels to be replenished with electrons at the clocking rates used, and this in turn could have affected the channel stop potentials near the output transistor. Given this experience, the importance of having a good ac ground via biased n^+ substrate contacts near the output transistor cannot be overstated.

From the discussion in the previous two sections, it is clear that to minimize surface potentials when fully depleted CCDs are operated at high substrate bias voltages it is beneficial to reduce p^+-p^+ spacings and to reduce the thickness of the field oxide. The potentials are still relatively large, and we describe in the next section techniques to reduce the electric fields resulting from these potentials.

C. Additional high-voltage considerations

In order to further reduce surface electric fields, we have simulated two junction termination techniques. Instead of the simple p^+ junctions shown in Fig. 5, the junctions shown in Fig. 6 contain a lightly doped p region that extends beyond the p^+ junctions and a metal field plate. The extended p region uses the same implant that forms the p-channels in the imaging array, so no extra processing steps are required to implement this feature. The nominal dose for this boron implant is $1.3 \times 10^{12} \text{ cm}^{-2}$, and this implant extends $2.5 \mu\text{m}$ past the p^+ junction in the HVC CCDs. The metal field plate is an extension of the metal contacting the p^+ region over the field oxide and extending beyond the p extension. In the HVC CCD design the metal extends beyond the p extension by $4 \mu\text{m}$.

Figure 13 b) shows the simulated electric fields along a horizontal line at a depth of $0.34 \mu\text{m}$ into the silicon for

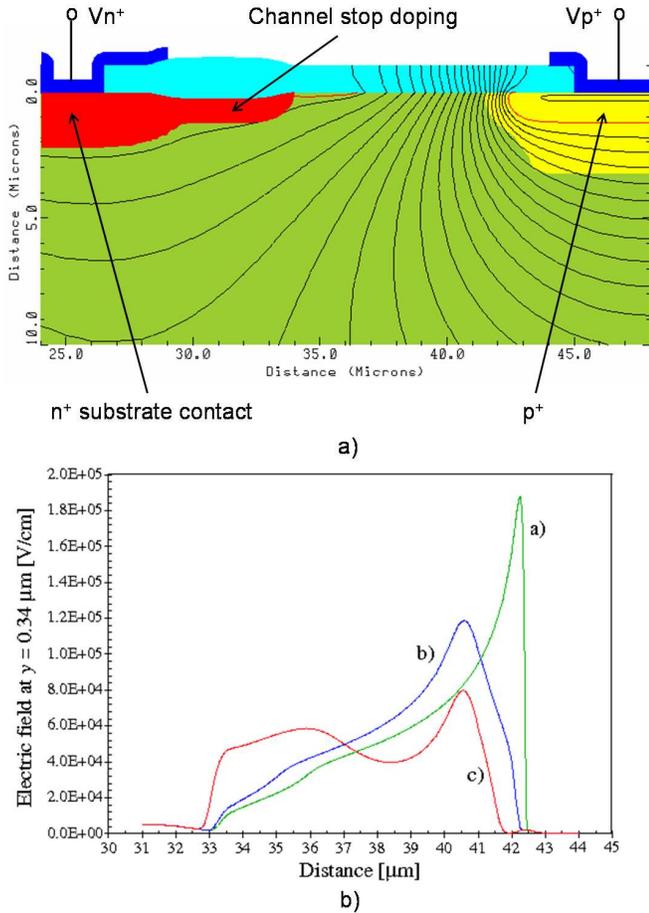


Fig. 13. a) 2-D simulation cross section showing the n⁺ contact at the top left of the structure biased at 40V, and the p⁺ junction biased at 0V. Equipotential lines spaced 2V apart are shown. The simulated substrate thickness was 200 μm. b) Electric field simulations for the structure shown in a) and in Fig. 6. The field is plotted along a 1-D horizontal line at a depth of 0.34 μm into the silicon. The x-axis values correspond to the cross section shown in a). Curve a) corresponds to the case of no p extension, i.e. the cross section shown in a) above. Curve b) is for the case where the p extension of Fig. 6 is present. Curve c) is the same as b) but with a metal field plate over the SiO₂ layer that extends beyond the p extension as in Fig. 6.

the cross section shown in Fig. 13 a) and with and without the junction termination methods shown in Fig. 6. For this simulation the n⁺ substrate contact was biased at 40V, V_{sub} was 100V, and the p⁺ junction was grounded. The substrate thickness in the simulation was 200 μm. In each case the p⁺-n⁺ spacing was 14 μm, and the channel stop region extends 4 μm to the right of the n⁺ implant edge. Curve a) corresponds to the case with no p extension or field plate, and b) and c) are the simulated fields for the case of the p extension and p extension with field plate, respectively. It is seen that the junction termination techniques are quite efficient at reducing the surface electric fields. For the HVC CCDs the p⁺ regions near the output transistors and imaging array always have the p extension, and also have the field plate whenever possible. The exceptions to the latter are the spacings between metal lines that carry signal and bias voltages past the p⁺ junctions.

Another feature that reduces surface electric fields is the use

of lightly doped, n-type regions that receive no ion implants between the p extensions and the channel stops as shown in Figs. 6 and 13 a). This creates a lateral p-i-n diode. The voltage dropped across the lightly doped region reduces the peak fields when compared to the case where the same reverse bias voltage is applied between the p⁺ and n⁺ electrodes without the lightly doped region. By selectively masking the channel and notch implants in the active region we are able to have surface regions with the extremely low doping of the substrate and take advantage of the lateral p-i-n diode structure.

This lightly doped region is prone to the formation of hole inversion layers, and this is eliminated by the polysilicon shield shown in Fig. 8. Metal lines crossing over the lightly doped regions can cause surface inversion if the potential on the metal line is sufficiently negative with respect to the nearby, grounded p⁺ regions. In the HVC CCDs the source follower transistor power supply voltage is nominally -22V, and the reset level is -12.5V. In addition, the output voltage of the source follower transistor is typically around -17V with no signal charge present. The threshold voltage for the case when the substrate is fully depleted before the onset of inversion is given by

$$V_T = V_{FB} + V_C - 2\phi_N - \frac{C_{sub}}{C_{ox}}(\phi_N - V_C + V_{sub}) - \frac{qN_{DY}N}{2C_{ox}} \quad (7)$$

where V_C is the channel potential for the source of holes, i.e. the grounded p⁺ region, and $2\phi_N$ is the band bending at inversion. The last two terms in Eq. 7 are relatively small, and the threshold voltage is dominated by the fixed oxide charge in the flatband voltage. For $N_F = 3 \times 10^{11}$ and a total oxide thickness under the metal of 1.25 μm, the fixed oxide term is about -17V. Therefore hole inversion is expected for at least the metal lines biased at -22V, and this has been verified by simulation. In order to avoid this, the metal lines carrying large negative voltages are routed over field-oxide regions, then over the grounded polysilicon shield thereby avoiding the crossing of these metal lines over any lightly doped regions.

In addition to lowering surface potentials, the proximity of the grounded p⁺ regions to the imaging area has other advantages. Figure 14 shows simulation cross sections generated by extending the cross section shown in Fig. 10 horizontally on both sides. A large volume consisting of the entire 200 μm thick substrate including 20 imaging array pixels and about 100 μm of silicon to the left of the p-channel regions is simulated. Figure 14 shows the simulated electric field lines for two cases, with the difference being the presence of a p⁺ region near the imaging array in Fig. 14 b) as is done in the HVC CCD. In addition, the substrate bias voltages used, 25 and 100V for Fig. 14 a) and b), respectively, approximate the usual operating voltage for the two types of CCDs. The field lines are specified in the simulator to begin at the surface in the imaging array and are spaced at a pixel pitch of 10.5 μm. In the bulk of the substrate the lines can distort from the ideal vertical lines due to the lateral extent of the depletion region from the p-channel pixels. For back-illuminated CCDs it is seen that the edge pixels do not faithfully reproduce the spatial

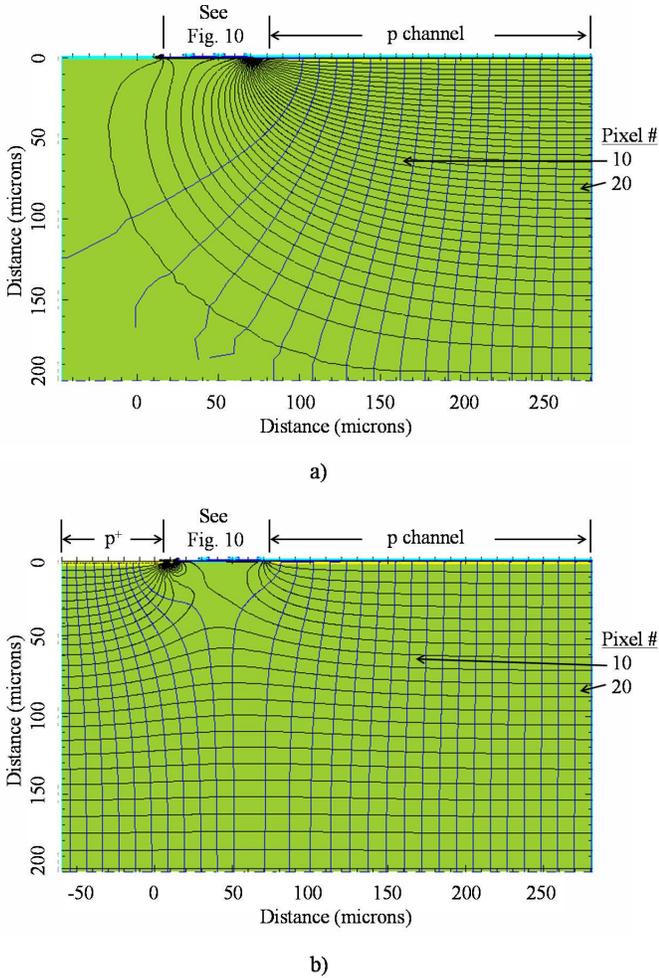


Fig. 14. Simulation cross sections illustrating the pixel distortion effect for pixels near the edge of the imaging array. A column of the CCD is approximated by the p-channel implant region that extends to the right edge of the structure. The region labeled “See Fig. 10” is shown in detail in Fig. 10. Equipotential and electric field lines are shown, with the latter being perpendicular to the equipotential lines and approaching the vertical towards the right side of the structure. a) The case for no p^+ region near the imaging area. The simulated substrate bias voltage was 25V and the equipotential spacing was 1V. b) The case when a grounded, p^+ region is near the imaging area. The simulated substrate bias voltage was 100V and the equipotential spacing is 5V.

coordinates of the image. This use of the nearby grounded p^+ region and the larger substrate bias voltage significantly reduces the number of distorted, edge pixels. Note that the Neumann boundary condition on the vertical edges of the simulation structure of Fig. 14 forces the electric field normal to the vertical edges to zero, and this could result in an underestimate of the actual distortion of the edge pixels. The other advantage of the p^+ junction near the imaging array is the ability of this junction to collect photo-generated holes that would otherwise be collected in the edge pixels.

D. Future efforts

We have recently developed other large-area, high-voltage compatible CCDs, including $15\ \mu\text{m}$ pixel devices with formats of $4\text{k} \times 2\text{k}$ and $4\text{k} \times 4\text{k}$ for use in ground-based-astronomy spectrographs. In addition, we have shown that for CCDs fabricated on sufficiently high-resistivity substrates that one can fully deplete the standard thickness, 650–675 μm thick, quality control CCDs from the foundry [24]. The ability to fully deplete thick substrates extends the quantum efficiency for hard x rays to the 10–15 keV range, and such devices could have application in direct detection of x rays at for example x-ray synchrotrons.

The use of fully depleted channel stops in the imaging area of the CCDs described here is contrary to the usual efforts in commercial CCD and CMOS imagers to suppress surface dark currents through the use of pinned photodiodes [27], virtual phase pixels [28], and multi-pinned phase CCDs [29]. Given the operation of the HVC CCDs at cryogenic temperatures the use of a depleted surface condition is acceptable since the dark-current generating energy levels can be filled with carriers with long emission time constants. We do observe some anomalies that we speculate are due to non-uniform filling of surface traps in the channel stop regions. For example, we sometimes see a small, approximately 1% response variation in a region localized to a few rows. We have empirical methods to eliminate such effects, but a better understanding of the problem would be useful. We plan to investigate this further.

IV. CONCLUSION

We have presented device design methods and experimental results for large format, fully depleted CCDs that can be operated at high substrate bias voltages. The large substrate bias enables good spatial resolution while maintaining high red response. The issues related to the operation of fully depleted CCDs at large substrate bias voltages have been described, and 2-D process and device simulation has been used to study these issues and guide the design.

APPENDIX A

DERIVATION OF THE 1-D POTENTIALS IN THE CHANNEL STOP REGION FOR A FULLY DEPLETED CCD

In the following we solve the 1-D Poisson equation for the channel stop region shown in Fig. 15. Poisson’s equation in the field-oxide region is

$$\frac{d^2V}{dy^2} = 0 \quad -d_{cs} < y < 0 \quad (\text{A1})$$

with boundary condition

$$V(-d_{cs}) = V_G - V_{FB} \quad (\text{A2})$$

In the channel stop the Poisson equation and boundary conditions are

$$\frac{d^2V}{dy^2} = \frac{-qN_{D,cs}}{\epsilon_{Si}} \quad 0 < y < y_{cs} \quad (\text{A3})$$

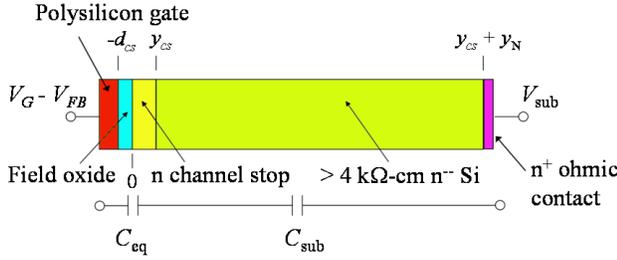


Fig. 15. CCD cross section in the channel stop region.

$$V(0^-) = V(0^+) \quad (A4)$$

$$\epsilon_{ox} \frac{dV}{dy}(0^-) = \epsilon_{Si} \frac{dV}{dy}(0^+) \quad (A5)$$

and finally for the substrate

$$\frac{d^2V}{dy^2} = \frac{-qN_D}{\epsilon_{Si}} \quad y_{cs} < y < (y_{cs} + y_N) \quad (A6)$$

$$V(y_{cs}^-) = V(y_{cs}^+) \quad (A7)$$

$$\frac{dV}{dy}(y_{cs}^-) = \frac{dV}{dy}(y_{cs}^+) \quad (A8)$$

$$V(y_{cs} + y_N) = V_{sub} \quad (A9)$$

Solving the above for the electrostatic potentials in the various regions yields

$$V(y) = V_G - V_{FB} - E_{ox}(y + d_{cs}) \quad -d_{cs} < y < 0 \quad (A10)$$

$$V(y) = V_G - V_{FB} - E_{ox} \left(\frac{\epsilon_{ox}}{\epsilon_{Si}} y + d_{cs} \right) - \frac{qN_{D,cs}}{2\epsilon_{Si}} y^2 \quad 0 < y < y_{cs} \quad (A11)$$

$$V(y) = V_{sub} + \frac{qN_D}{2\epsilon_{Si}} ((y_N + y_{cs})^2 - y^2) + \left(\frac{qy_{cs}}{\epsilon_{Si}} (N_{D,cs} - N_D) + \frac{\epsilon_{ox}}{\epsilon_{Si}} E_{ox} \right) (y_N + y_{cs} - y) \quad y_{cs} < y < (y_{cs} + y_N) \quad (A12)$$

After some lengthy algebra E_{ox} , the electric field in the field-oxide, is determined to be

$$E_{ox} = -[V_{sub} - (V_G - V_{FB}) + \frac{qN_{D,cs}}{\epsilon_{Si}} \left(\frac{y_{cs}^2}{2} + y_{cs}y_N \right) + \frac{qN_D}{2\epsilon_{Si}} y_N^2] / \left[\frac{\epsilon_{ox}}{\epsilon_{Si}} (y_N + y_{cs}) + d_{cs} \right] \quad (A13)$$

For $y_N \gg y_{cs}$, d_{cs} and $N_{D,cs} \gg N_D$, E_{ox} becomes

$$E_{ox} \approx -\frac{V_{sub} - (V_G - V_{FB}) + qN_{D,cs}y_N y_{cs} / \epsilon_{Si}}{y_N \epsilon_{ox} / \epsilon_{Si}} \quad (A14)$$

For typical numbers the last term in the numerator is much larger than the voltage terms. For example, if $N_{D,cs}y_{cs}$ is the nominal HVC CCD channel stop dose of $1 \times 10^{12} \text{ cm}^{-2}$ and y_N is 200 μm , then the last term in the numerator is about 3200, which is much larger than V_{sub} and $(V_G - V_{FB})$. As a result, to a good approximation E_{ox} is given by

$$E_{ox} \approx -qN_{D,cs}y_{cs} / \epsilon_{ox} \quad (A15)$$

Also of interest is the substrate bias voltage required to fully deplete the channel stop and substrate, and this is given by

$$V_D = V_G - V_{FB} + \frac{q}{2\epsilon_{Si}} (N_{cs}y_{cs}^2 + N_D y_N^2) + \frac{q}{C_{ox}} (N_{cs}y_{cs} + N_D y_N (1 + \frac{C_{ox}}{C_{cs}})) \quad (A16)$$

where C_{cs} is ϵ_{Si}/y_{cs} .

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REFERENCES

- [1] G. Aldering *et al.*, "Overview of the Supernova/Acceleration Probe (SNAP)," *Proc. SPIE*, **4835**, pp. 146–157, 2002.
- [2] S. Perlmutter, "Supernovae, dark energy, and the accelerating Universe," *Phys. Today*, **56**, pp. 53–60, 2003.
- [3] S.E. Holland, D.E. Groom, N.P. Palaio, R.J. Stover, and M. Wei, "Fully depleted, back-illuminated charge-coupled devices fabricated on high-resistivity silicon," *IEEE Trans. Elec. Dev.*, **50**, pp. 225–238, 2003.
- [4] A. Karcher *et al.*, "Measurement of lateral charge diffusion in thick, fully depleted, back-illuminated CCDs," *IEEE Trans. Nucl. Sci.*, **51**, pp. 2231–2237, 2004.
- [5] J. Fairfield *et al.*, "Improved spatial resolution in thick, fully depleted CCDs with enhanced red sensitivity," *IEEE Trans. Nucl. Sci.*, **53**, pp. 3877–3881, 2006.
- [6] S.E. Holland *et al.*, "A 200 × 200 CCD image sensor fabricated on high-resistivity silicon," *IEDM Technical Digest*, pp. 911–914, 1996.
- [7] B.E. Burke *et al.*, "CCD soft-x-ray detectors with improved high- and low-energy performance," *IEEE Trans. Nucl. Sci.*, **51**, pp. 2322–2327, 2004.
- [8] H. Suzuki, M. Muramatsu, K. Yamamoto, S. Miyazaki, and Y. Kamata, "Development of the fully-depleted thick back-illuminated CCD by Hamamatsu," *2007 IEEE Nucl. Sci. Symp. Conf. Rec.*, pp. 4581–4585, Honolulu, HI, 2007.
- [9] Y. Kamata *et al.*, "Recent developments of the fully depleted back-illuminated CCD developed by Hamamatsu," *Proc. SPIE*, **6276**, Orlando, FL, 2006.
- [10] P. Jorden *et al.*, "Commercialisation of full depletion scientific CCDs," *Proc. SPIE*, **6276**, Orlando, FL, 2006.
- [11] R.A. Bredthauer, J.H. Pinter, J.R. Janesick, and L.B. Robinson, "Notch and large area CCD imagers," *Proc. SPIE*, **1447**, pp. 310–315, 1991.
- [12] DALSA Semiconductor, 18 Airport Blvd., Bromont, Quebec, Canada.
- [13] S.E. Holland, K.S. Dawson, N.P. Palaio, J. Saha, N.A. Roe, and G. Wang, "Fabrication of back-illuminated, fully depleted charge-coupled devices," *Nucl. Instrum. Meth. Phys. Res. A*, **579**, pp. 653–657, 2007.
- [14] M.H. Fabricius, C.J. Bebek, D.E. Groom, A. Karcher, and N.A. Roe, "Quantum efficiency characterization of back-illuminated CCDs Part II: Reflectivity measurements," *Proc. SPIE*, **6068**, pp. 101–111, 2006.
- [15] N.A. Roe *et al.*, "Radiation-tolerant, red-sensitive CCDs for dark energy investigations," *Nucl. Instrum. Meth. Phys. Res. A*, **572**, pp. 526–527, 2007.

- [16] D.E. Groom, C.J. Bebek, M.H. Fabricius, A. Karcher, W.F. Kolbe, N.A. Roe, and J. Steckert, "Quantum efficiency characterization of back-illuminated CCDs Part I: The Quantum Efficiency Machine," *Proc. SPIE*, **6068**, pp. 133–143, 2006.
- [17] J.R. Janesick, "*Scientific charge-coupled devices*", SPIE Press, 2001.
- [18] R. Newman, "Visible light from a silicon p-n junction," *Phys. Rev.*, **100**, pp. 700–703, 1955.
- [19] A.G. Chynoweth and K.G. McKay, "Photon emission from avalanche breakdown in silicon," *Phys. Rev.*, **102**, pp. 369–376, 1956.
- [20] N. Akil, S.E. Kerns, D.V. Kerns, Jr., A. Hoffman, and J-P. Charles, "Photon generation by silicon diodes in avalanche breakdown," *Appl. Phys. Lett.*, **73**, pp. 871–872, 1998.
- [21] Y.C. Kao and E.D. Wolley, "High-voltage planar p-n junctions," *Proceedings of the IEEE*, vol. 55, no. 8, pp. 1409–1414, August 1967.
- [22] M.S Adler, "Theory and breakdown voltage for planar devices with a single field limiting ring," *IEEE Trans. Elec. Dev.*, vol. 24, no. 2, pp. 107-113, February 1977.
- [23] V. Boisson, M. Le Helley, and J.P. Chante, "Analytical expression for the potential of guard rings of diodes operating in the punchthrough mode," *IEEE Trans. Elec. Dev.*, vol. 32, no. 4, pp. 838-840, April 1985.
- [24] S.E. Holland *et al.*, "High-voltage compatible, fully depleted CCDs," *Proc. SPIE*, **6276**, Orlando, Fl, 2006.
- [25] J.-I. Nishizawa, T. Terasaki, and J. Shibata, "Field-effect transistor versus analog transistor (static induction transistor)," *IEEE Trans. Elec. Dev.*, **22**, pp. 186–197, 1975.
- [26] A.G.M. Strollo and P. Spirito, "A self-consistent model for the SIT DC characteristics," *IEEE Trans. Elec. Dev.*, **38**, pp. 1943–1951, 1991.
- [27] N. Teranishi, A. Kohono, Y. Ishihara, E. Oda, and K. Arai, "No image lag photodiode structure in the interline CCD image sensor," *IEDM Technical Digest*, pp. 324-327, 1982.
- [28] J. Hyneczek, "Virtual phase CCD technology," *IEDM Technical Digest*, pp. 611-614, 1979.
- [29] J. Janesick, T. Elliott, M. Blouke, and B. Corrie, "Charge-coupled device pinning technologies," *Proc. SPIE*, **1071**, pp. 153–169, 1989.